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HIGH SPEED, RADIATION HARD MRAM BUFFER

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Abstract—Radiation hardened nonvolatile memory has many applications in DoD military, space systems, MILSATCOM, and commercial space systems. However, most nonvolatile memory components that exist today do not fully meet the requirements of these applications. A novel, low power, Magnetoresistive Random Access Memory (MRAM), that uses a Sandwich-Spin Dependent Tunneling (SSDT) memory bit and that meets all of the application requirements, is described. The SSDT bit combines a sandwich storage structure with tunneling magnetoresistance readout. A single, bi-polar write current is used to write the bit. A write select transistor, in the memory cell, selects a single bit for writing - thereby eliminating half-select conditions. Antiferromagnetic coupling in the sandwich film minimizes the required switching field, leading to low write currents - as low as 4 mA seen in 2 µm devices and 0.8 mA predicted for an 0.6 µm device. A two bit, differential cell, is being used to design a 1k buffer memory, that will use SDT memory elements that have been radiation tested to over 1 Mrad.

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1. INTRODUCTION

Magnetoresistive RAM (MRAM), a nonvolatile memory technology that uses one of several types of magnetoresistive films for both data storage and readout, was originally developed as a replacement for plated wire memory - for use in military applications that required a radiation hard memory. The original MRAM used Anisotropic Magneto-Resistance (AMR) films, which were tested and shown to be radiation hard in the memory application. Current MRAM developments generally use a Spin Dependent Tunneling (SDT) magnetoresistive film. While the SDT based MRAM is expected to exhibit the same radiation hardness, in the storage-readout element, as the AMR based MRAM does, the current MRAM development efforts are focused on commercial markets. As such, the radiation characteristics of the SDT elements have not been a concern, and the circuits have not been developed in a radiation hard process. In radiation hard applications, a high speed, radiation hard, nonvolatile SDT MRAM could be used as a distributed memory to provide nonvolatile storage of coefficients and register data, or it could be used as the main storage device. Another application, that utilizes the high speed, nonvolatile characteristics of such a memory, is in high speed data recorders. Data recorders measuring shock or high speed events may require large amounts of data to obtain high resolution measurements as well as make these measurements over a period of time. Presently, FLASH technology is the only nonvolatile solid state technology that has both high storage density and immunity to battery failure - but it lacks sufficient write speed to provide real time storage of the data stream that is generated by a high speed data acquisition system. The SDT MRAM can be used as an intermediate buffer between the data acquisition circuitry and the FLASH memory, compensating for the low write speed of the FLASH by buffering the data stream during the FLASH's block write. Radiation test data, to over 1 Mrad for SDT devices, is presented, along with the design of a high speed, radiation hard, buffer MRAM. This buffer memory combines the inherently radiation hard SDT memory element with **SOI** circuitry

2. MRAM BUFFER SOLUTION

An MRAM design using Sandwitch-Spin Dependent Tunneling (SSDT) technology with unique film and circuit design, is being developed by NVE. This design has very low power and has a high-speed write, which is especially important for buffer applications in battery, powered equipment. High speed read and write operation are essential for buffer application, where the buffer memory must first accumulate data while a slow FLASH

memory is performing a write cycle, and then quickly flush the data to the FLASH page buffer.

Since the MRAM SSDT memory design is compatible with standard semiconductor processing, the memory can be integrated with a PLD or an ASIC which is used to control the operation and provide the data buffering for the high shock data recorder. It also can be used as a stand alone component such as a small serial I^2C EEROM equivalent component. Since MRAM has been shown to be inherently radiation resistant in AMR based MRAM devices, radiation hard components using the SSDT design can be constructed which would be useful in satellite and missile applications.

3. HARDENING MRAM COMPONENTS

Ensuring reliable operation of electronics working in an environment with radiation is in most cases a complicated, time consuming and an expensive task. Normal commercial electronics components are not qualified to work in environments with radiation and specially designed and/or specially qualified components are required above a radiation dose of a few hundred Rad.

Radiation effects on electronics are normally divided into 3 different categories according to their effect on the electronic components:

Total ionizing dose: Total Ionizing Dose (TID) effects on modern integrated circuits cause the threshold voltage of MOS transistors to change because of trapped charges in the silicon dioxide gate insulator. For sub-micron devices these trapped charges can potentially "escape" by tunneling effects. Leakage currents are also generated at the edge of (N)MOS transistors and potentially between neighbor N-type diffusions. Commercial digital CMOS processes can normally stand a few Krad without a significant increase in power consumption. Modern sub-micro technologies tend to be more resistant to total dose effects than older technologies. High performance analog devices may though potentially be affected at quite low doses. Total dose is measured in Rad or Gray (1 Gray = 100 Rad.)

Displacement damage: Hadrons may displace atoms (therefore called displacement effect) in the silicon lattice of active devices and thereby affect their function. Bipolar devices and especially optical devices (e.g. Lasers, LEDs, Optical receivers, Opto-couplers) may be very sensitive to this effect. CMOS integrated circuits are normally not considered to suffer degradation by displacement damage. The total effect of different types of hadrons at different energies are normalized to 1 Mev Neutrons using the NIEL (Non Ionizing Energy Loss) equivalent.

Single event effects: Single Event Effects (SEE) refer to the fact that it is not a cumulative effect but an effect related to single individual interactions in the silicon. Highly ionizing particles can directly deposit enough charge locally in the silicon to disturb the function of electronic circuits. Energetic Hadrons (> ~20Mev) can by nuclear interactions within the component itself generate recoils that also deposits sufficient charge locally to disturb the correct function. The different SEE effects are normally characterized by an energy threshold and a sensitivity cross-section at energies well above the threshold.

Single event upset: The deposited charge is sufficient to flip the value of a digital signal. Single Event Upsets (SEU) normally refer to bit flips in memory circuits (RAM, Latch, flip-flop) but may also in some rare cases directly affect digital signals in logic circuits.

Single event latchup: Bulk CMOS technologies (not Silicon On Insulator) have parasitic bipolar transistors that can be triggered by a locally deposited charge to generate a kind of short circuit between the power supply and ground. CMOS processes are made to prevent this to occur under normal operating conditions but a local charge deposition from a traversing particle may potentially trigger this effect. Single event latchup may be limited to a small local region or may propagate to affect large parts of the chip. The large currents caused by this short circuit effect can permanently damage components if they are not externally protected against the large short circuit current and the related power dissipation.

Single event burnout: Single event burnout refers to destructive failures of power MOSFET transistors in high power applications. For HEP applications this destructive failure mechanism is normally associated to failures in the main switching transistors of switching mode power supplies.

Since MRAM cells have been shown to be inherently radiation resistant, focus can be placed on the design and fabrication of the supporting electronics. Fabrication processes will use Peregrine Semiconductor Corporation’s rad-hard process. Their process utilizes a proprietary Ultra Thin Silicon (UTSI) process for fabricating rad-hard integrated circuits using silicon-on-sapphire (SOS) wafers. They are able to process 0.35 µM lithographys, which will mesh well with the lithographys that NVE is currently using. Peregrine discussed their Rad-Hard capabilities and presented a road map at GOMAC 2001[6].

4. MRAM BUFFER MEMORY

NVE's MRAM buffer memory uses a write select transistor in each cell, and a sandwich storage structure. The select transistor eliminates the half-select condition that non-addressed cells experience in other MRAM memories - which eliminates write cycle disturbs of neighbor cells.

The sandwich storage element provides flux closure during writes - minimizing the required write energy. Also, with an anti-ferromagnetically coupled sandwich, sensitivity to external disturb fields is greatly reduced.

Most MRAM schemes use a 2D current selection scheme to read and/or write the cell. The original MRAM [1] concept and the Pseudo Spin Valve (PSV) [2] concept both use magnetic 2D selection, i.e. two, usually orthogonal, currents, for both the read operation and the write operation. In both cases, all of the cells on both the row and the column that contain the addressed cell will experience a half-select condition. Similarly, Spin Dependent Tunneling (SDT, a.k.a. Magnetic Tunnel Junction, or MTJ) memories [3,4,5] use 2D selection when writing a cell. Again, this creates a half-select condition for all cells on the same row and column as the addressed cell. In all cases, the half-select condition increases the likelihood of a disturb, and places stringent requirements on the uniformity of the magnetic characteristics of the cells.

The MRAM buffer memory uses an SDT memory cell that has a sandwich film on one side of the tunnel junction, and that contains two select transistors - one that is used during readout and one that is used during writing. Figure 1 illustrates this cell structure, showing schematically both the SDT structure and the select transistors. To write the cell, the write select transistor is turned on, and a write current flows through the sandwich portion of the cell. This write current flows in the plane of the SDT film. For a read operation, only the read select transistor is turned on, and a small tunneling current is passed through the cell in order to generate a readout voltage. For a given read current, the readout voltage will depend upon the alignment between the magnetizations of the magnetic films that are adjacent to the top and bottom surfaces of the tunneling barrier.

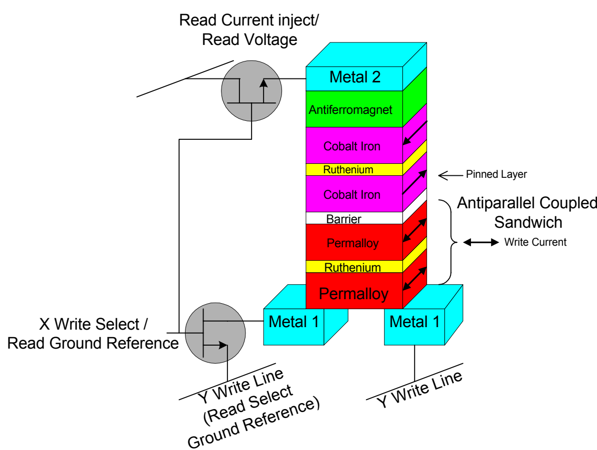


Figure 1. Schematic illustration of the SSDT memory cell. The magnetic sandwich, below the tunnel barrier, is the storage element, and is written with in-plane current. Vertical conduction, through the tunnel barrier, is used for readout.

For the cell shown in Figure 1, the write current only flows through the selected cell. Since no write current flows through adjacent, non-selected cells, the half-select condition that exists in other MRAM is eliminated. Without a half-select condition, the switching uniformity requirement is eased considerably. As long as the write current is set high enough to write the cell that has the highest write threshold, all cells in the memory can be written without disturbing a non-selected cell. Compared to the switching uniformity that is required for a 2D selection scheme, this single current selection scheme greatly improves the manufacturability of the memory. It is the combination of the sandwich storage element and the write select transistor that allows the single current selection scheme to work. In other MRAM cells, the write current flows through a separate current conductor - not through the storage element. The need for the separate conductor, combined with the sensitivity of other MRAM designs to disturb fields, makes it impractical to use the single current selection scheme with the other types of MRAM.

The second key feature of the innovative SSDT buffer memory is significantly lower write current than other MRAM cells. This lower write current is due to the closed flux switching behavior of the anti-ferromagnetically coupled Ruthenium sandwich film that forms the storage element in the SDT buffer cell. Because switching involves a pair of magnetic films that are always aligned antiparallel to one another, the high demagnetization fields that are encountered during switching of a single layer film are avoided. Thus, smaller switching fields, and therefore smaller switching currents, are needed.

The SSDT cell will be used in a Two Junction per Cell (2JC) architecture, that uses a relatively simple latch cell circuit with one SSDT junction in each of the two halves of the latch cell. This architecture is shown schematically in Figure 2. The two SSDT devices are written to opposite states - one high resistance and one low resistance. To read the memory, the latch is momentarily shorted, so that both outputs are at the same potential, and then released. When the short is removed, the different resistance that is presented to the two halves of the latch, by the oppositely written SSDT junctions, causes the latch output to rapidly drive to a known logic level based on which SSDT junction is in a higher resistance state. This architecture is very fast and robust since the two cells provide high signal and act as local "references" for each other - there is no need to match closely to a reference cell that may be located a relatively large distance away.

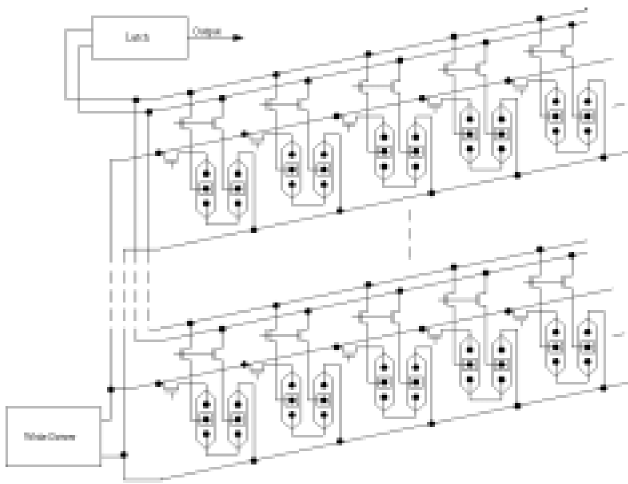


Figure 2. Schematic diagram of the 2JC memory architecture. The 2 SSDT elements in each cell self-reference one another for readout - requiring only a simple latch.

The 2JC memory architecture appears to be a latch similar to that of SRAM. However, in radiation environments, it can be seen that the MRAM is more immune to upsets. If one of the transistors in the SRAM latch is upset, the data will be lost. Where as in the case of the 2JC latch, the data is contained in the SSDT cells, not the associated transistor. If one of those transistors is upset, it will have no effect on the data.

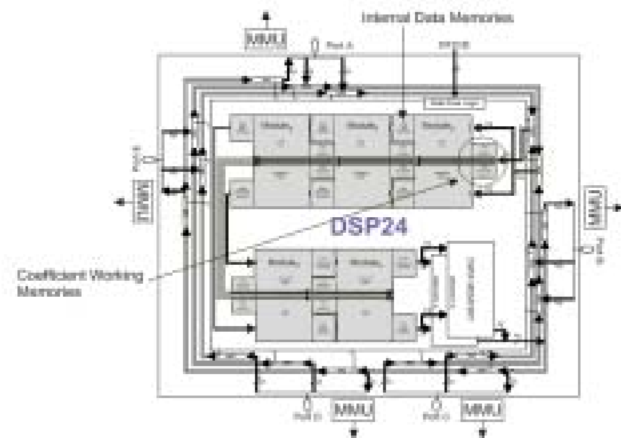
5. MILITARY APPLICATIONS

Although the basic concept of magnetoresistive random access memory (MRAM) has led to working memory cells on silicon and to limited numbers of working MRAM chips, demonstration of practical manufacturability of MRAM has not been reported. One of the major stumbling blocks to producing MRAM is the stringent magnetic uniformity requirement that the 2D memory organization places on the MRAM cell, an organization which all serious MRAM developments currently employ. Staying with a 2D approach may delay or even preclude the practical manufacturing of MRAM. Because defense applications really need fast and truly nonvolatile random access memories, this could represent a significant difficulty for the Department of Defense. A Phase I program with Kirtland AFB entitled “Radiation-Hardened Non-Volatile RAM” addressed the radiation resistance of MRAM SDT cells and alternative circuit designs to eliminate the problems of disturbs and uniformity found in 2D MRAM memory architectures. Novel memory cells and circuit architectures now make possible the development of a reliable and manufacturable radiation hard MRAM component that will satisfy the on-going need of the military and space community.

A preliminary demonstration of the resistance of SDT cells to radiation was completed during the Phase I effort with Kirtland AFB. SDT junctions were irradiated in a ^{60}Co source at GD-IS. After a total dose of 1 Mrad, the vast majority had no catastrophic failures or significant parameter shifts. The devices that were available for this testing did not have on-chip ESD protection circuits, and were very susceptible to test induced damage - so there were some parameter shifts and failures seen in both the control group and radiation group. Statistically, the changes/failures in the radiation group were no different than that of the control group.

The nonvolatile, radiation hard MRAM has broad application in the military, ranging from space and defense applications, in which the radiation hardness of MRAM is of paramount importance, to terrestrial applications in which high speed write and nonvolatility are most critical. An example of the latter is in buffer applications. In a data recorder application, a modest sized MRAM can be used to buffer a high speed data stream between the data acquisition system and a relatively slow-write nonvolatile mass storage. In this case, the last data points that are obtained before power goes out, due to damage from the event of interest, could be very critical to understanding the event. Normally, these data points would be lost. With an MRAM buffer, however, this data would still be retained. Other applications of a buffer memory could be in a radiation environment where the MRAM could act as a high speed buffer between an electronic system and a lower speed, nonvolatile storage such as a magnetic hard drive.

Applications for MRAM extend beyond these buffer applications to include distributed and embedded applications in radiation hard systems, such as for military satellites. Not only will the MRAM provide radiation hard data storage, but it can enable savings in system power and size. Consider the Digital Signal Processor (DSP), that is essential to many of the tasks that are performed by satellite systems. Use of embedded MRAM in a DSP can increase the speed of the DSP as well as shrink the die size. In a typical DSP, coefficients are daisy chained forward through the chip. By incorporating MRAM, the coefficients can be pre-stored at the needed location - this is shown in Fig. 3, which illustrates where various memory components are located in the DSP. With the pre-stored coefficients, the speed of the DSP is increased. Also, because the MRAM is nonvolatile, the chip can be powered down when not in use. This will save on system power without affecting speed - since the coefficients will not need to be reloaded when the chip is powered up again. In addition to coefficient storage, Fig. 3 lists other memory components within the DSP that could advantageously be implemented in MRAM - taking advantage of MRAM's high speed, nonvolatility.



Current DSP24 Memory Functions	MRAM Candiate
Coefficient/Template/Window Memory	Yes
Internal Data Memories	No
Program Memory	Yes
Memory Management Unit (MMU) Seeds	Yes
Coefficient Working Memories	Yes

Figure 3. Block diagram of a DSP and a table of DSP memory functions that could potentially be implemented in MRAM.

PROBLEM → ▪ The Coefficients and Their Management Require Large Silicon Areas to Allow them To Keep Up with the Data as it Propagates through the Chip.

▪ The DSP24 Shown Below Contains Five (5) Cores, A Larger DSP Chip May Have Ten (10) Cores and Thus Suffer from Twice as Many Coefficient Required Areas.

SOLUTION → ▪ The Green Area in Coefficient #2 Represents the Estimated Area That would be Required for an Equivalent MRAM Pre-stored Coefficient Structure, about 10% of the Current Structure.

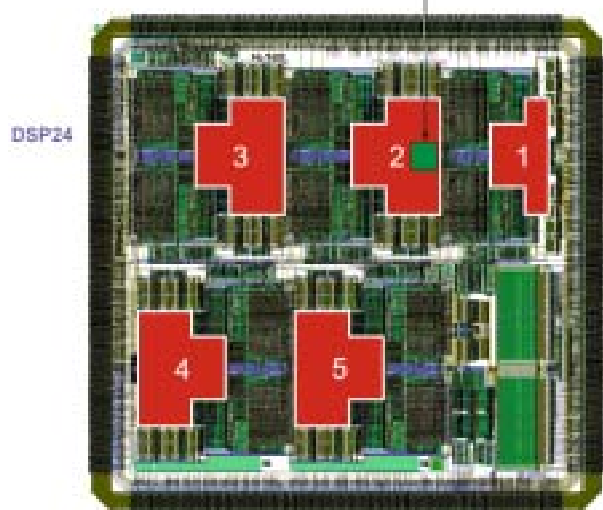


Figure 4. Illustration of the anticipated IC area savings that result from using MRAM in a DSP.

In addition to increasing speed/performance and lowering power consumption, the use of MRAM in a DSP can reduce the die size. Figure 4 illustrates the area savings that are anticipated from using MRAM in an existing, high performance DSP. In Fig. 4, the existing coefficient storage and management area is outlined - and the area required for MRAM replacement for one of these blocks is outlined within one of the existing coefficient areas. The MRAM area is only about 10% of the existing coefficient storage area.

6. CONCLUSIONS

The development of new MRAM components, that use the SSDT cell and memory architecture that is presented in this paper, will eliminate the problems of volatility in main memory, buffer, and embedded applications that require small, high speed, low power, random access memory devices. In addition, with its inherent resistance to radiation effects, it has many applications in radiation environments. Initial devices with sizes on the order of 1 Kbyte will be developed, with sizes evolving up through 16 megabit as production refinements are completed. Small buffer MRAM devices will be incorporated into PLDs giving them high-speed nonvolatile storage which is not available today. Embedded MRAM can be used to provide power, speed, and size enhancements to DSPs.

7. ACKNOWLEDGEMENTS

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