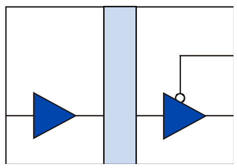
NVE CORPORATION

IL710H-3E

High-Rel Single-Channel Data Coupler

Functional Diagram



Truth Table

V_I	$V_{\overline{OE}}$	V_O
L	L	L
H	L	H
L	H	Z
H	H	Z

Features

- High Speed: 150 Mbps typical
- −55 °C to 125 °C
- 2500 V_{RMS} isolation voltage
- 100 kV/µs common mode transient immunity
- Excellent magnetic immunity
- 44000 year barrier life
- High-reliability NiPdAu-Ag leadframe
- IEC 60747-17 (VDE 0884-17):2021-10 certified; UL 1577 recognized
- Low outgassing
- No carrier or clock for low EMI emissions and susceptibility
- Extended 2.7 to 5.5 volt supply range
- 500 V_{RMS} IS-to-IS intrinsically safe
- 1.2 mA/channel typical quiescent current
- 300 ps typical pulse width distortion
- 100 ps pulse jitter
- SOIC8 package

Applications

- High-reliability industrial applications
- Space and aerospace applications
- Ground loop elimination
- Serial communication
- Logic level shifting

Description

The IL710H-3E is a high-reliability version of NVE's industry-leading IL700-Series isolated data couplers.

The devices are manufactured with NVE's patented* spintronic Giant Magnetoresistive (GMR) technology, which provides the ultimate in reliability and inherent radiation tolerance.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

To meet high-reliability industrial requirements, the "H" version uses a NiPdAu-Ag leadframe, has the full −55 °C to 125 °C military temperature range, and has verified low outgassing in accordance with NASA specifications.

*U.S. Patent numbers 5,831,426; 6,300,617 and others.

Rev. A

Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55		150	°C	
Junction Temperature	T_J	–55		150	°C	
Ambient Operating Temperature(1)	T_A	–55		125	°C	
Supply Voltage	V_{DD1}, V_{DD2}	–0.5		7	V	
Input Voltage	V_I	–0.5		V_{DD1}+0.5	V	
Input Voltage	$V_{\overline{OE}}$	–0.5		V_{DD2}+0.5	V	
Output Voltage	V_O	–0.5		V_{DD2}+0.5	V	
Output Current Drive	I_O			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	T_A	–55		125	°C	
Junction Temperature	T_J	–55		150	°C	
Supply Voltage	V_{DD1}, V_{DD2}	2.7		5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD1}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	μs	

Safety and Approvals

IEC 60747-17 (VDE 0884-17):2021-10 (Basic Isolation; VDE File Number 5016933-4880-0001):

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating: 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit
- Working Voltage (V_{IORM}; pollution degree 2): 700 V_{RMS}

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180°C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

UL 1577 (Component Recognition Program File Number E207481)

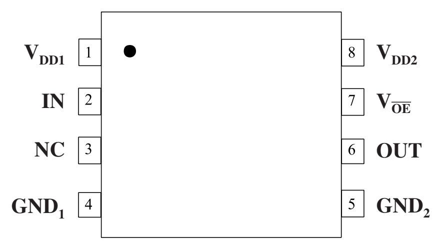
- 2500 V isolation rating
- Each part tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute.

Soldering Profile

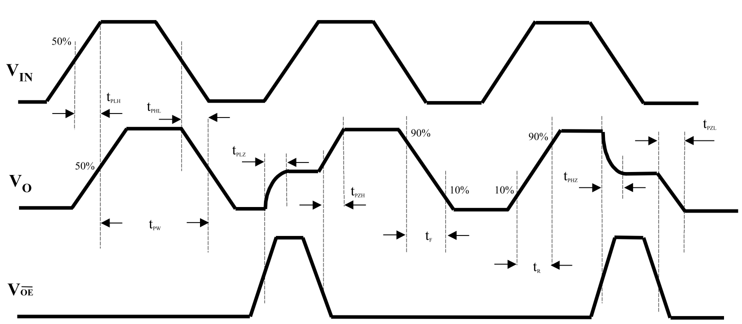
Per JEDEC J-STD-020C, MSL 1

Pin Connections

1	V_{DD1}	Supply voltage
2	IN	Data In
3	NC	No internal connection
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT	Data Out
7	$V_{\overline{OE}}$	Output enable (internally held low with 100 kΩ)
8	V_{DD2}	Supply voltage



Timing Diagram



Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_{PLZ}	Propagation Delay, Low to High Impedance
t_{PZH}	Propagation Delay, High Impedance to High
t_{PHZ}	Propagation Delay, High to High Impedance
t_{PZL}	Propagation Delay, High Impedance to Low
t_R	Rise Time
t_F	Fall Time

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3.3 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current	I_{DD1}		8	10	µA	
Output Quiescent Supply Current	I_{DD2}		1.2	1.75	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD}−0.1	V_{DD}		V	I_O = −20 µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.5	0.8		I_O = 4 mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 3.3 V)						
Maximum Data Rate		130	140		Mbps	C_L = 15 pF
Pulse Width(7)	PW	10	7.5		ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	C_L = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t_{PHZ}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t_{PLZ}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t_{PZH}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t_{PZL}		3	5	ns	C_L = 15 pF
Pulse Width Distortion(2)	PWD		1	3	ns	C_L = 15 pF
Pulse Jitter(10)	t_J		100		ps	C_L = 15 pF
Propagation Delay Skew(3)	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		2	4	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		2	4	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)(4)	$\|CM_H\|,\|CM_L\|$	100	150		kV/µs	Per IEC 60747
Dynamic Power Consumption(6)						
Input side			140	240	µA/Mbps/ch	
Output side			20	40		

Magnetic Field Immunity(8) (V_{DD2} = 3 V, 3 V < V_{DD1} < 5.5 V)						
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

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5 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current	I_{DD1}		10	15	µA	
Output Quiescent Supply Current	I_{DD2}		1.8	2.5	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD}−0.1	V_{DD}		V	I_O = −20 µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.5	0.8		I_O = 4 mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 5 V)						
Maximum Data Rate		130	150		Mbps	C_L = 15 pF
Pulse Width(7)	PW	10	7.5		ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	C_L = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t_{PHZ}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t_{PLZ}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t_{PZH}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t_{PZL}		3	5	ns	C_L = 15 pF
Pulse Width Distortion(2)	PWD		0.3	3	ns	C_L = 15 pF
Propagation Delay Skew(3)	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)(4)	$\|CM_H\|,\|CM_L\|$	100	150		kV/µs	Per IEC 60747
Dynamic Power Consumption(6)			200	340	µA/Mbps	

Magnetic Field Immunity(8) (V_{DD2}= 5 V, 3 V < V_{DD1}< 5.5 V)						
Power Frequency Magnetic Immunity	H_{PF}		3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		4500		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}		4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

Insulation Specifications

Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)			4.04			mm	
Total Barrier Thickness (internal)			0.012	0.013		mm	
Leakage Current[5]				0.2		μA	240 V_{RMS}, 60 Hz
Barrier Resistance[5]		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance[5]		C_{IO}		1.1		pF	f = 1 MHz
Comparative Tracking Index		CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
	DC		1500			V_{DC}	
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	θ_{JA}		134		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	θ_{JC}		10		°C/W	
Power Dissipation	P_D			675	mW	

Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H and CM_L are the maximum common mode voltage slew rates that can be applied with the outputs remaining stable and within V_{OL} and V_{OH} specifications.
5. Device is considered a two terminal device: pins 1–4 shorted and pins 5–8 shorted.
6. Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 7.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 7).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

Typical Performance Graphs

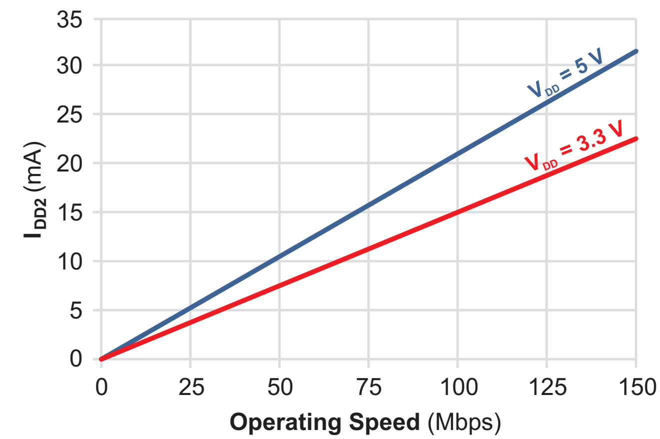


Figure 1. Supply current vs. operating speed.

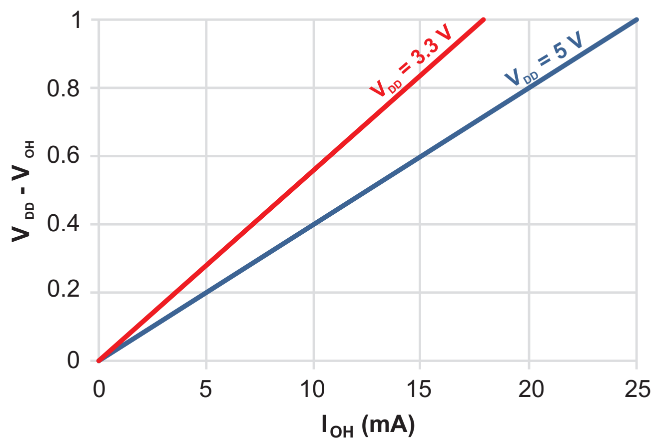


Figure 2. Typical high output voltage vs. load.

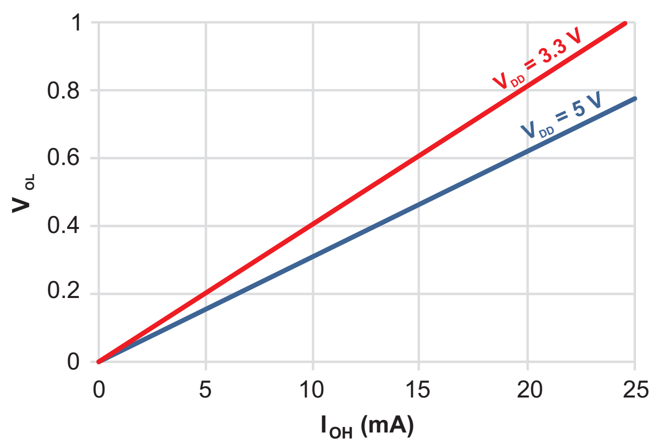
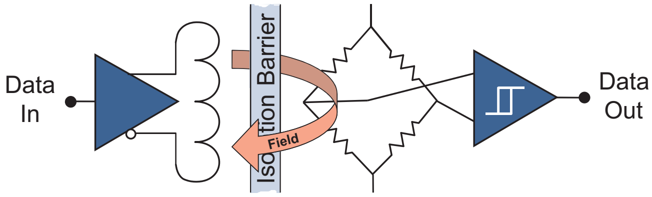


Figure 3. Typical low output voltage vs. load

Application Information

Isolator Operation

An equivalent circuit is shown below:



Isolator Signal Path

The GMR isolator signal path starts with a buffered input signal that is driven through an ultraminiature coil. This generates a small magnetic field that changes the electron spin polarization of GMR resistors, which are configured as a Wheatstone bridge. The change in spin polarization of the resistors creates a bridge voltage which drives an output comparator to construct an isolated version of the input signal.

Small Size, High Speed, and Low EMI

The coil, GMR, and circuitry are integrated to allow small packages. GMR is inherently high speed and low distortion, and unlike transformers, does not rely on energy transfer, so power is low and EMI emissions are minimal.

High Magnetic Immunity

GMR provides large signals which improve magnetic immunity, and the Wheatstone bridge configuration cancels ambient common-mode magnetic fields, further enhancing immunity to external magnetic fields.

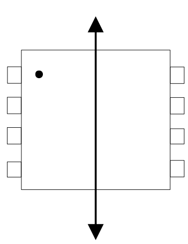
Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

IL700-Series Isolators have the lowest EMC footprint of any isolation technology. The Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. These isolators are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

Dynamic Power Consumption

IL700-Series Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Power Supply Decoupling

Both power supplies should be decoupled with 0.1 µF typical (0.047 µF minimum) capacitors as close as possible to the V_{DD} pins. Ground planes for both GND_1 and GND_2 are highly recommended for data rates above 10 Mbps.

Signal Status on Start-Up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

$$\text{PWD\%} = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

For example, with data rates of 12.5 Mbps:

$$\text{PWD\%} = \frac{3\text{ ns}}{80\text{ ns}} \times 100\% = 3.75\%$$

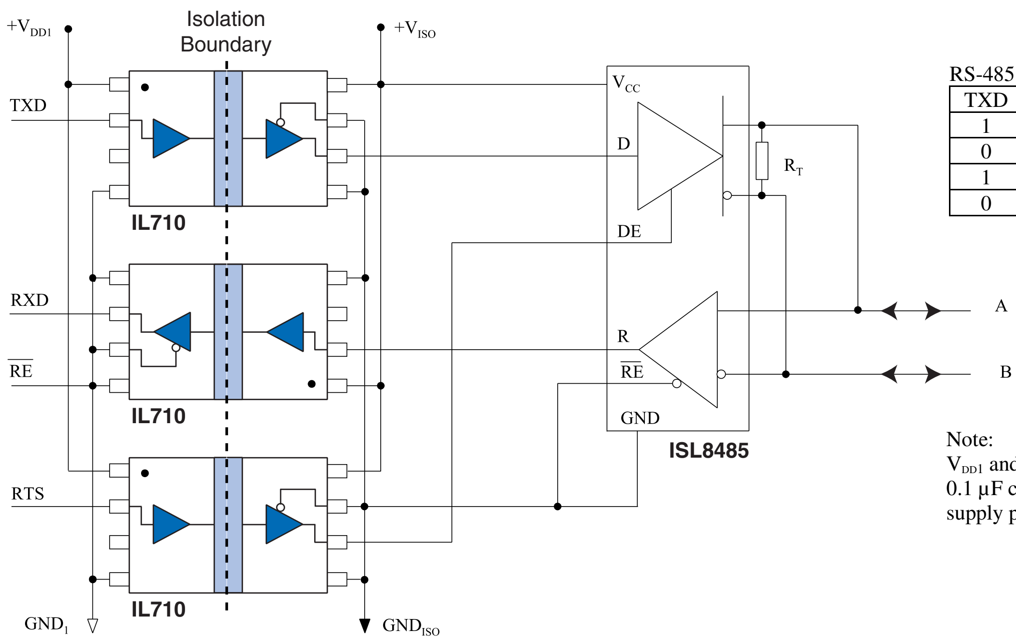
This figure is almost **three times** better than any available optocoupler with the same temperature range, and **two times** better than any optocoupler regardless of published temperature range. The isolators will run to nearly 35 Mbps within the PROFIBUS 10% Pulse Width Distortion limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in an IL700 Isolator is only 3 ns, which is **ten times** better than any optocoupler. IL700 Isolators have a maximum propagation delay skew of 6 ns, which is **five times** better than any optocoupler.

Application Diagrams

Isolated PROFIBUS / RS-485

NVE offers a unique line of single-chip isolated PROFIBUS/RS-485 transceivers, but as this circuit illustrates, IL710 isolators can also be used as part of multi-chip designs using non-isolated PROFIBUS transceivers:



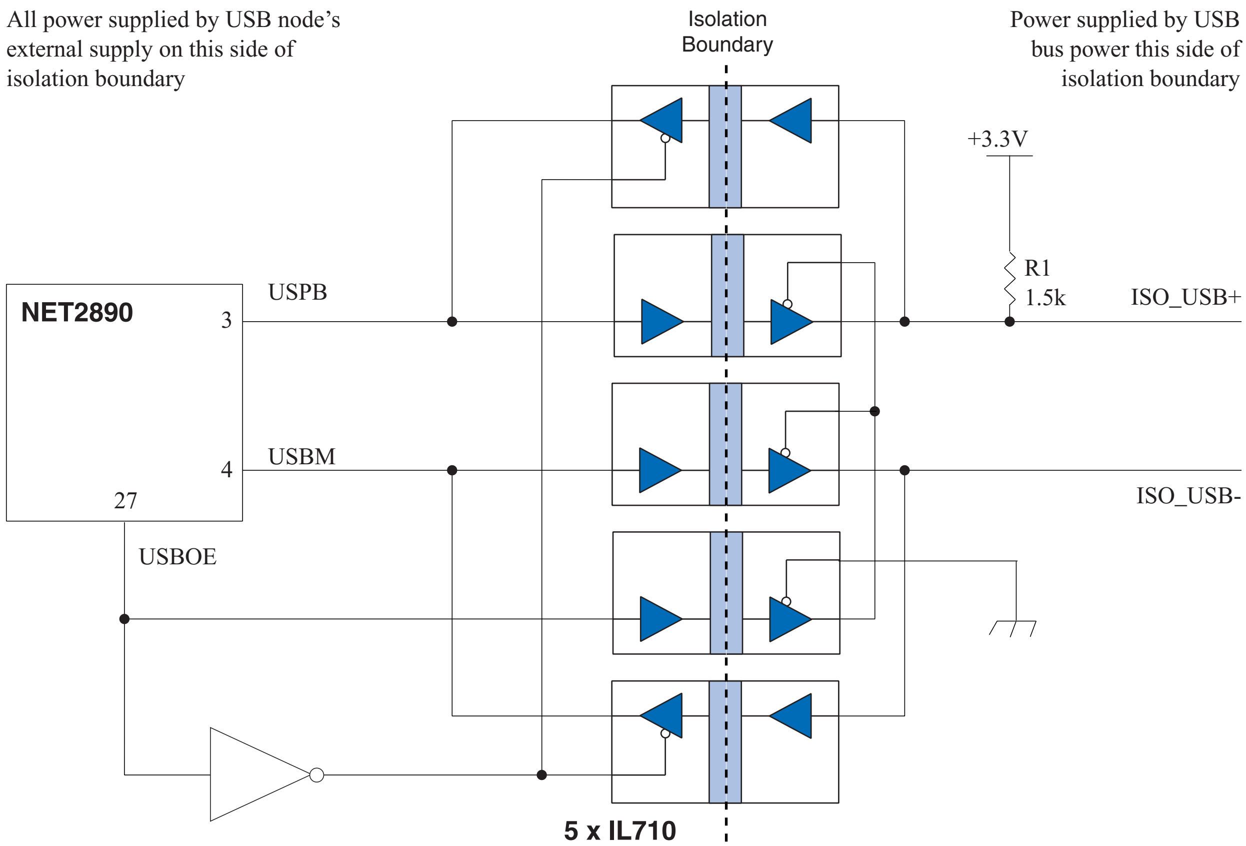
RS-485 Truth Table

TXD	RTS	A	B	RXD
1	0	Z	Z	X
0	0	Z	Z	X
1	1	1	0	1
0	1	0	1	0

Note:
V_{DD1} and V_{ISO} should be decoupled with 0.1 µF ceramic capacitors at IL710 supply pins.

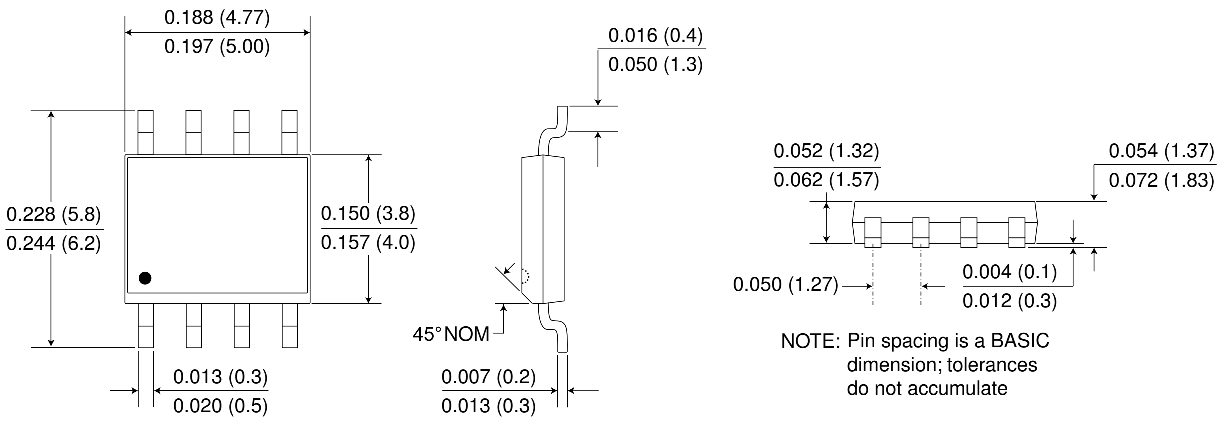
Isolated USB

In this circuit, power is supplied by USB bus power on one side of the isolation barrier, and the USB node's external supply on the other side of the barrier. IL700 Isolators are specified with just 3 ns worst-case pulse width distortion:



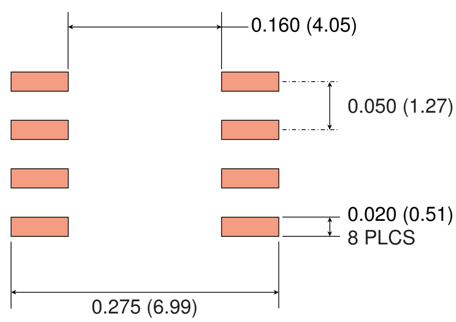
Package Drawing (SOIC8)

Dimensions in inches (mm); scale = approx. 5X



Recommended Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Revision History

ISB-DS-001-IL710H-A March 2024	Change • Initial release.

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