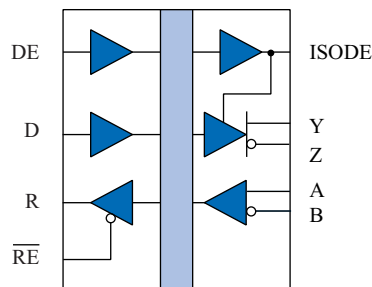


## Low-Cost Isolated RS485/RS422 Transceiver

### Functional Diagram



**IL3022**

#### IL3022 Receiver

RE	R	V <sub>(A-B)</sub>
H	Z	X
L	H	≥ 200 mV
L	L	≤ -200 mV
L	H	Open

#### IL3022 Driver

DE	D	V <sub>(Y-Z)</sub>
L	X	Z
H	H	≥ 2 V
H	L	≤ -2 V

H = High Level, L = Low Level  
X = Irrelevant, Z = High Impedance

### Features

- 4 Mbps data rate
- Full duplex
- Supports up to 32 nodes
- 3 V to 5 V power supplies
- 50 kV/μs typ.; 30 kV/μs min. common mode transient immunity
- Low quiescent supply current
- 44000 year barrier life
- 7 kV bus ESD protection
- Low EMC footprint
- Thermal shutdown protection
- -40 °C to +85 °C temperature range
- Meets or exceeds ANSI RS-485 and ISO 8482:1987(E)
- 2500 V<sub>RMS</sub> isolation voltage per UL 1577
- IEC 60747-17 (VDE 0884-17):2021-10 certified; UL 1577 recognized
- 0.3" True 8<sup>TM</sup> mm 16-pin SOIC package

### Applications

- Factory automation
- Industrial control networks
- Building environmental controls
- Equipment covered under IEC 61010-1 Edition 3

### Description

The IL3022 is a galvanically isolated, high-speed, full-duplex differential bus transceiver, designed for bidirectional data communication on balanced transmission lines. The device uses NVE's patented\* spintronic Giant Magnetoresistance (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The wide-body package provides true 8 mm creepage.

The IL3022 delivers at least 1.5 V into a 27 Ω load for excellent data integrity over long cable lengths. The device is compatible with 3.3 V input supplies, allowing interface to standard microcontrollers without additional level shifting.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs feature a "fail-safe if open" design, ensuring a logic high R-output if A/B are floating.

## Absolute Maximum Ratings<sup>(6)</sup>

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	$T_S$	-55		150	°C	
Junction Temperature	$T_J$	-55		150	°C	
Voltage Range at A or B Bus Pins		-8		12.5	V	
Supply Voltage <sup>(1)</sup>	$V_{DD1}, V_{DD2}$	-0.5		7	V	
Digital Input Voltage		-0.5		$V_{DD} + 0.5$	V	
Digital Output Voltage		-0.5		$V_{DD} + 1$	V	
ESD (all bus nodes)		7			kV	HBM

## Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	$V_{DD1}$ $V_{DD2}$	3.0 4.5		5.5 5.5	V	
Ambient Operating Temperature	$T_A$	-40		85	°C	
Junction Temperature	$T_J$	-40		100	°C	
Input Voltage at any Bus Terminal (separately or common mode)	$V_I$ $V_{IC}$			12 -7	V	
High-Level Digital Input Voltage	$V_{IH}$	2.4 3.0		$V_{DD1}$	V	$V_{DD1} = 3.3\text{ V}$ $V_{DD1} = 5.0\text{ V}$
Low-Level Digital Input Voltage	$V_{IL}$	0		0.8	V	
Differential Input Voltage <sup>(2)</sup>	$V_{ID}$			+12 / -7	V	
High-Level Output Current (Driver)	$I_{OH}$			60	mA	
High-Level Digital Output Current (Receiver)	$I_{OH}$			8	mA	
Low-Level Output Current (Driver)	$I_{OL}$	-60			mA	
Low-Level Digital Output Current (Receiver)	$I_{OL}$	-8			mA	
Digital Input Signal Rise and Fall Times	$t_{IR}, t_{IF}$					DC Stable

## Safety and Approvals

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**IEC 60747-17 (VDE 0884-17):2021-10** (Basic Isolation; VDE File Number 5016933-4880-0001)

- Working Voltage ( $V_{IORM}$ ) 600  $V_{RMS}$  (848  $V_{PK}$ ); basic insulation; pollution degree 2
- Isolation voltage ( $V_{ISO}$ ) 2500  $V_{RMS}$
- Transient overvoltage ( $V_{IOTM}$ ) 4000  $V_{PK}$
- Surge rating 4000 V
- Each part tested at 1590  $V_{PK}$  for 1 second, 5 pC partial discharge limit
- Samples tested at 4000  $V_{PK}$  for 60 sec.; then 1358  $V_{PK}$  for 10 sec. with 5 pC partial discharge limit
- Working Voltage 600  $V_{RMS}$

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	$T_S$	180	$^{\circ}C$
Safety rating power (180 $^{\circ}C$ )	$P_S$	270	mW
Supply current safety rating (total of supplies)	$I_S$	54	mA

**UL 1577** (Component Recognition Program File Number E207481)

Each part tested at 3000  $V_{RMS}$  (4240  $V_{PK}$ ) for 1 second; each lot sample tested at 2500  $V_{RMS}$  (3530  $V_{PK}$ ) for 1 minute

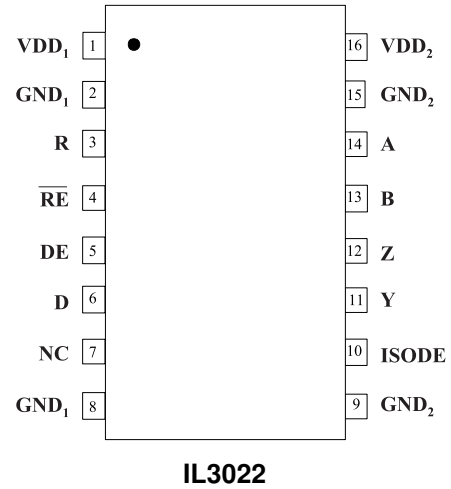
## Soldering Profile

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Per JEDEC J-STD-020C, MSL 1

## IL3022 Pin Connections

1	V <sub>DD1</sub>	Input Power Supply
2	GND <sub>1</sub>	Input Power Supply Ground Return (pin 2 is internally connected to pin 8)
3	R	Output Data from Bus
4	$\overline{RE}$	Read Data Enable (if $\overline{RE}$ is high, R = high impedance)
5	DE	Drive Enable
6	D	Data Input to Bus
7	NC	No Internal Connection
8	GND <sub>1</sub>	Input Power Supply Ground Return (pin 8 is internally connected to pin 2)
9	GND <sub>2</sub>	Output Power Supply Ground Return (pin 9 is internally connected to pin 15)
10	ISODE	Isolated DE Output for use in Profibus applications where the state of the isolated drive enable node needs to be monitored
11	Y	Y Bus (Drive – True)
12	Z	Z Bus (Drive – Inverse)
13	B	B Bus (Receive – Inverse)
14	A	A Bus (Receive – True)
15	GND <sub>2</sub>	Output Power Supply Ground Return (pin 15 is internally connected to pin 9)
16	V <sub>DD2</sub>	Output Power Supply



## Driver Section

Electrical Specifications (T <sub>min</sub> to T <sub>max</sub> and V <sub>DD</sub> = 4.5 V to 5.5 V unless otherwise stated)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Output voltage	V <sub>O</sub>			V <sub>DD</sub>	V	I <sub>O</sub> = 0
Differential Output Voltage <sup>(2)</sup>	V <sub>OD1</sub>			V <sub>DD</sub>	V	I <sub>O</sub> = 0
Differential Output Voltage <sup>(2)</sup>	V <sub>OD3</sub>	1.5	2.3	5	V	R <sub>L</sub> = 27 Ω, V <sub>DD</sub> = 4.5 V
Change in Magnitude of Differential Output Voltage <sup>(3)</sup>	Δ V <sub>OD1</sub>		±0.01	±0.2	V	R <sub>L</sub> = 27 Ω or 50 Ω
Common Mode Output Voltage	V <sub>OC</sub>			3	V	R <sub>L</sub> = 27 Ω or 50 Ω
Change in Magnitude of Common Mode Output Voltage <sup>(3)</sup>	Δ V <sub>OC1</sub>		±0.01	±0.2	V	R <sub>L</sub> = 27 Ω or 50 Ω
Output Current	I <sub>O</sub>			1 -0.8	mA	Output Disabled, V <sub>O</sub> = 12 V <sub>O</sub> = -7
High Level Input Current	I <sub>IH</sub>			10	μA	V <sub>I</sub> = 3.5 V
Low Level Input Current	I <sub>IL</sub>			-10	μA	V <sub>I</sub> = 0.4 V
Absolute  Short-circuit Output Current	I <sub>OS</sub>			250	mA	-7 V < V <sub>O</sub> < 12 V

## Receiver Section

Electrical Specifications (T <sub>min</sub> to T <sub>max</sub> and V <sub>DD</sub> = 4.5 V to 5.5 V unless otherwise stated)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Positive-going Input Threshold Voltage	V <sub>IT+</sub>			0.2	V	-7 V < V <sub>CM</sub> < 12 V
Negative-going Input Threshold Voltage	V <sub>IT-</sub>	-0.2			V	-7 V < V <sub>CM</sub> < 12 V
Hysteresis Voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )	V <sub>HYS</sub>		70		mV	V <sub>CM</sub> = 0 V, T = 25°C
High Level Digital Output Voltage	V <sub>OH</sub>	V <sub>DD</sub> - 0.2	V <sub>DD</sub>		V	V <sub>ID</sub> = 200 mV I <sub>OH</sub> = -20 μA
Low Level Digital Output Voltage	V <sub>OL</sub>			0.2	V	V <sub>ID</sub> = -200 mV I <sub>OH</sub> = 20 μA
High-impedance-state output current	I <sub>OZ</sub>			±1	μA	V <sub>O</sub> = 0.4 to (V <sub>DD2</sub> - 0.5) V
Line Input Current	I <sub>I</sub>			1 -0.8	mA	V <sub>I</sub> = 12 V V <sub>I</sub> = -7 V
Input Resistance	R <sub>I</sub>	12			kΩ	

## Power Consumption

T <sub>min</sub> to T <sub>max</sub> and V <sub>DD2</sub> = 5 V unless otherwise stated						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Controller-Side Quiescent Current V <sub>DD1</sub> = 3.3 V V <sub>DD1</sub> = 5 V	I <sub>DD1</sub>		3 4	4 6	mA	f <sub>IN</sub> = 0 Hz
Bus-Side Quiescent Supply Current	I <sub>DD2</sub>		5	16	mA	Outputs Enabled; R <sub>T</sub> = ∞; f <sub>IN</sub> = 0 Hz
Controller-Side Dynamic Supply Current	I <sub>DD1</sub>		0.22		mA/Mbps	V <sub>DD1</sub> = 3.3 V
Bus-Side Dynamic Supply Current	ΔI <sub>DD2</sub> /Δf <sub>IN</sub>		1 0.8			R <sub>T</sub> = ∞ R <sub>T</sub> = 60 Ω

## Switching Characteristics

V <sub>DD1</sub> = 5 V, V <sub>DD2</sub> = 5 V						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Data Rate		4			Mbps	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF
Propagation Delay <sup>(4)</sup>	t <sub>PD</sub>		48	150	ns	V <sub>O</sub> = -1.5 to 1.5 V, C <sub>L</sub> = 15 pF
Pulse Skew <sup>(5)</sup>	t <sub>SK(P)</sub>		6	15	ns	V <sub>O</sub> = -1.5 to 1.5 V, C <sub>L</sub> = 15 pF
Output Enable Time To High Level	t <sub>PZH</sub>		33	50	ns	C <sub>L</sub> = 15 pF
Output Enable Time To Low Level	t <sub>PZL</sub>		33	50	ns	C <sub>L</sub> = 15 pF
Output Disable Time From High Level	t <sub>PHZ</sub>		33	50	ns	C <sub>L</sub> = 15 pF
Output Disable Time From Low Level	t <sub>PLZ</sub>		33	50	ns	C <sub>L</sub> = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	CM <sub>H</sub>  , CM <sub>L</sub>	30	50		kV/μs	V <sub>CM</sub> = 1500 V <sub>DC</sub> t <sub>TRANSIENT</sub> = 25 ns
V <sub>DD1</sub> = 3.3 V, V <sub>DD2</sub> = 5 V						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Data Rate		4			Mbps	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF
Propagation Delay <sup>(4)</sup>	t <sub>PD</sub>		48	150	ns	V <sub>O</sub> = -1.5 to 1.5 V, C <sub>L</sub> = 15 pF
Pulse Skew <sup>(5)</sup>	t <sub>SK(P)</sub>		6	20	ns	V <sub>O</sub> = -1.5 to 1.5 V, C <sub>L</sub> = 15 pF
Output Enable Time To High Level	t <sub>PZH</sub>		33	50	ns	C <sub>L</sub> = 15 pF
Output Enable Time To Low Level	t <sub>PZL</sub>		33	50	ns	C <sub>L</sub> = 15 pF
Output Disable Time From High Level	t <sub>PHZ</sub>		33	50	ns	C <sub>L</sub> = 15 pF
Output Disable Time From Low Level	t <sub>PLZ</sub>		33	50	ns	C <sub>L</sub> = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	CM <sub>H</sub>  , CM <sub>L</sub>	30	50		kV/μs	V <sub>CM</sub> = 1500 V <sub>DC</sub> t <sub>TRANSIENT</sub> = 25 ns

## Magnetic Field Immunity<sup>(7)</sup>

V <sub>DD1</sub> = 5 V, V <sub>DD2</sub> = 5 V						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Power Frequency Magnetic Immunity	H <sub>PF</sub>		3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H <sub>PM</sub>		4500		A/m	t <sub>p</sub> = 8μs
Damped Oscillatory Magnetic Field	H <sub>OSC</sub>		4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(8)</sup>	K <sub>X</sub>		2.5			
V <sub>DD1</sub> = 3.3 V, V <sub>DD2</sub> = 5 V						
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Power Frequency Magnetic Immunity	H <sub>PF</sub>		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H <sub>PM</sub>		2000		A/m	t <sub>p</sub> = 8μs
Damped Oscillatory Magnetic Field	H <sub>OSC</sub>		2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(8)</sup>	K <sub>X</sub>		2.5			

## Insulation Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)		8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)		0.012	0.013		mm	
Barrier Resistance	R <sub>IO</sub>		>10 <sup>14</sup>		Ω	500 V
Barrier Capacitance	C <sub>IO</sub>		7		pF	f = 1 MHz
Leakage Current			0.2		μA <sub>RMS</sub>	240 V <sub>RMS</sub> , 60 Hz
Comparative Tracking Index	CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC		1000		V <sub>RMS</sub>	At maximum operating temperature
	DC		1500		V <sub>DC</sub>	
Barrier Life			44000		Years	100°C, 1000 V <sub>RMS</sub> , 60% CL activation energy

## Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	$\theta_{JA}$		67		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	$\theta_{JC}$		12			
Junction–Ambient Thermal Resistance	$\theta_{JA}$		46			2s2p PCB in free air per JESD51
Junction–Case (Top) Thermal Resistance	$\theta_{JC}$		9			
Power Dissipation	$P_D$			1500	mW	

## Notes:

1. All voltages are with respect to network ground except differential I/O bus voltages.
2. Differential input/output voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
3.  $\Delta V_{OD}$  and  $\Delta V_{OC}$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from one logic state to the other.
4. Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
5. Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel.
6. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
7. The relevant test and measurement methods are given in the Electromagnetic Compatibility section.
8. External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin.”

### **Electrostatic Discharge Sensitivity**

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

### **Power Supply Decoupling**

$V_{DD1}$  and  $V_{DD2}$  should be bypassed with 0.1  $\mu\text{F}$  typical (0.047  $\mu\text{F}$  minimum) capacitors as close as possible to the  $V_{DD}$  pins.

### **Maintaining Creepage**

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

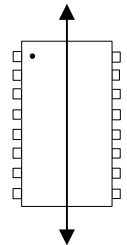
### **DC Correctness**

The IL3022 incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power up, the bus outputs will follow the Function Table shown on page 1 of this datasheet. The DE input should be held low during power-up to eliminate false drive data pulses from the bus. An external power supply monitor to minimize glitches caused by slow power-up and power-down transients is not required.

### **Electromagnetic Compatibility**

The IL3022 is fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

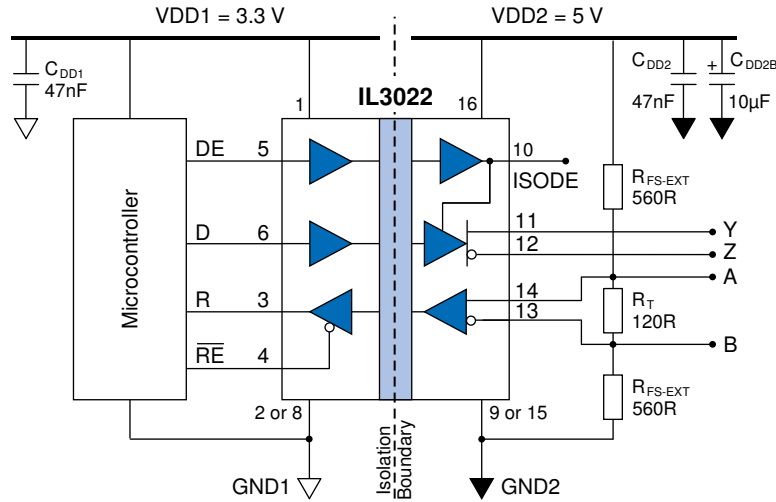
The IsoLoop Isolator’s Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EM immunity. Immunity to external magnetic fields is even higher if the field direction is “end-to-end” (rather than to “pin-to-pin”) as shown at right.





**Application Information**

The following figure shows typical connections to a microcontroller. The schematic includes typical termination and fail-safe resistors, and power supply decoupling capacitors:



**Typical connections.**

*Receiver Features*

The receiver includes a “fail-safe if open” function that guarantees a high level output if the receiver inputs are unconnected (floating). The receiver output “R” has tri-state capability via the active low  $\overline{RE}$  input.

*Driver Features*

The RS-422 driver is differential output and delivers at least 1.5 V across a 54  $\Omega$  load. Drivers feature low propagation delay skew to maximize bit width and minimize EMI. Drivers have tri-state capability via the active-high DE input.

*Receiver Data Rate, Cables and Terminations*

The IL3022 is intended for networks up to 4,000 feet (1,200 m), but the maximum data rate decreases as cable length increases. Twisted pair cable should be used in all networks since they tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers.

**Fail-Safe Operation**

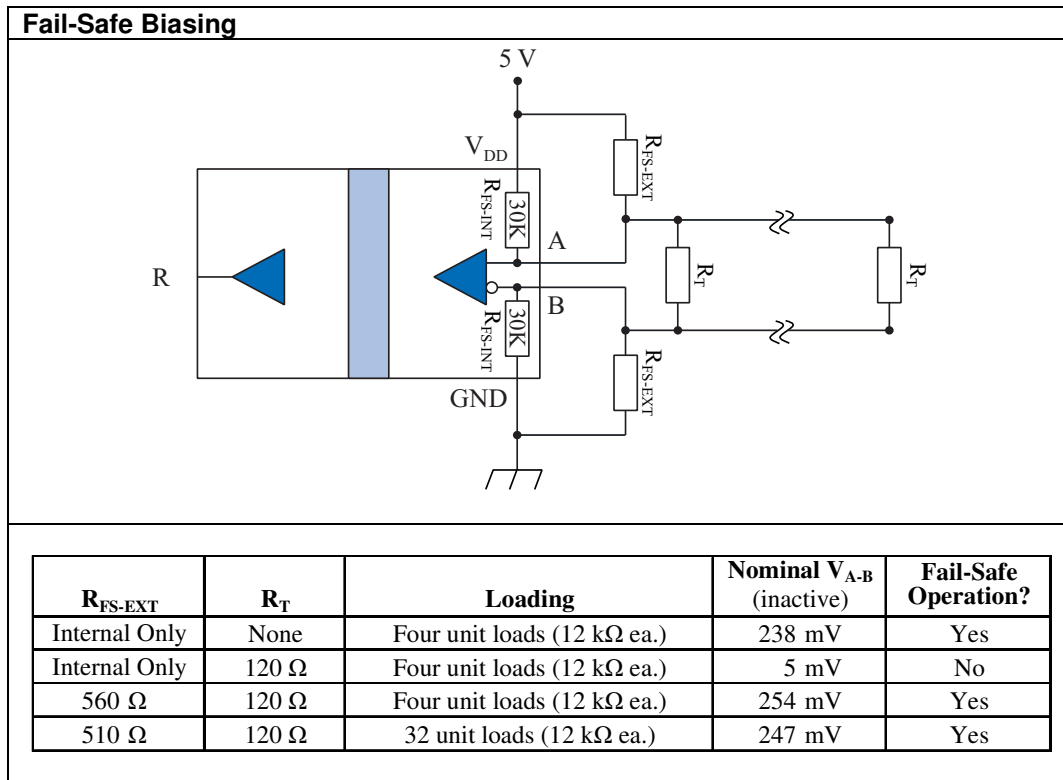
“Fail-safe operation” is defined here as the forcing of a logic high state on the “R” output in response to an open-circuit condition between the “A” and “B” lines of the bus, or when no drivers are active on the bus.

Proper biasing can ensure fail-safe operation, that is a known state when there are no active drivers on the bus. IL3000-Series Isolated Transceivers include internal pull-up and pull-down resistors of approximately 30 kΩ in the receiver section (R<sub>FS-INT</sub>; see figure below). These internal resistors are designed to ensure failsafe operation but only if there are no termination resistors. The entire V<sub>DD</sub> will appear between inputs “A” and “B” if there is no loading and no termination resistors, and there will be more than the required 200 mV with up to four RS-422 worst-case Unit Loads of 12 kΩ. Many designs operating below 1 Mbps or less than 1,000 feet are unterminated. Termination resistors may not be necessary for very low data rates and very short cable runs because reflections have time to settle before data sampling, which occurs at the middle of the bit interval.

In busses with low-impedance termination resistors, however, the differential voltage across the conductor pair will be close to zero with no active drivers. In this case the state of the bus is indeterminate, and the idle bus will be susceptible to noise. For example, with 120 Ω termination resistors (R<sub>T</sub>) on each end of the cable, and four Unit Loads (12 kΩ each), without external fail-safe biasing resistors the internal pull-up and pull-down resistors will produce a voltage between inputs “A” and “B” of only about 5 mV. This is not nearly enough to ensure a known state. External fail-safe biasing resistors (R<sub>FS-EXT</sub>) at one end of the bus can ensure fail-safe operation with a terminated bus. Resistors should be selected so that under worst-case power supply and resistor tolerances there is at least 200 mV across the conductor pair with no active drivers to meet the input sensitivity specification of the RS-422 standard.

Using the same value for pull-up and pull-down biasing resistors maintains balance for positive- and negative going transitions. Lower-value resistors increase inactive noise immunity at the expense of quiescent power consumption. Note that each Unit Load on the bus adds a worst-case loading of 12 kΩ across the conductor pair, and 32 Unit Loads add 375 Ω worst-case loading. The more loads on the bus, the lower the required values of the biasing resistors.

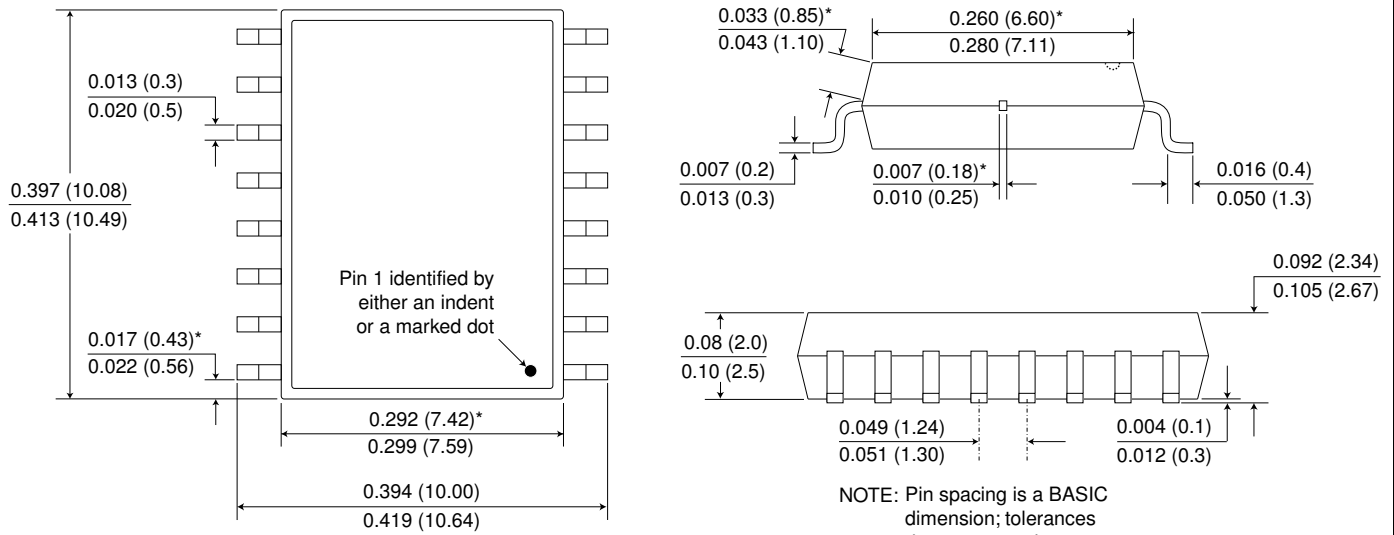
In the example with two 120 Ω termination resistors and four Unit Loads, 560 Ω external biasing resistors provide more than 200 mV between “A” and “B” with adequate margin for power supply variations and resistor tolerances. This ensures a known state when there are no active drivers. Other illustrative examples are shown in the table below:



**Package Drawing**

**0.3" 16-pin SOIC Package**

Dimensions in inches (mm); scale = approx. 5X

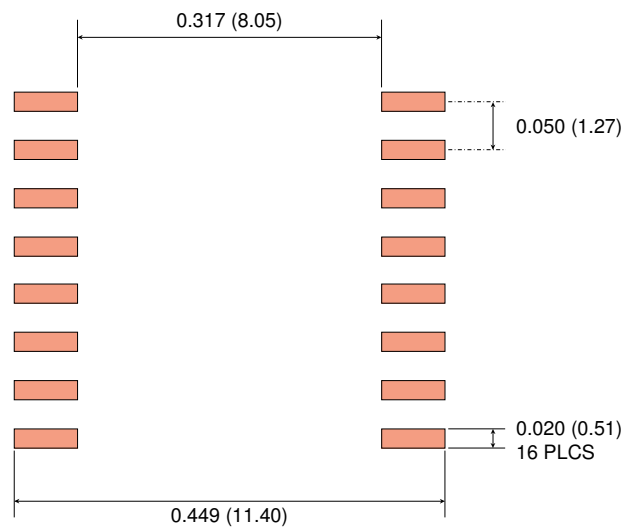


\*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

**Recommended Pad Layout**

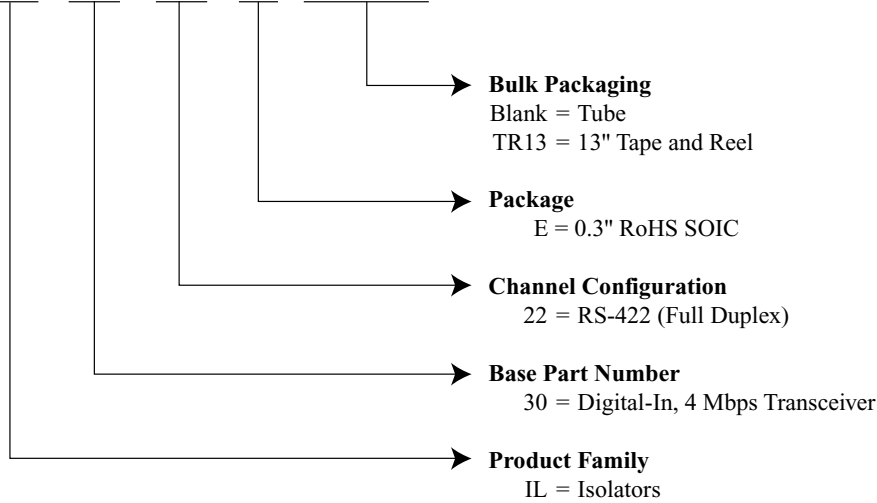
**0.3" 16-pin SOIC Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



## Ordering Information and Valid Part Numbers

IL 30 22 E TR13



**Valid Part Numbers**

IL3022E  
IL3022E TR13



## Revision History

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**ISB-DS-001-IL3022-B**  
**October 2022**

### Changes

- Upgrade to VDE 0884-17 (p. 3).
- Separate power consumption specifications section; added dynamic power consumption (p. 5).
- Revised thermal characteristics (p. 7).
- Updated EMC standards.
- Deleted minimum magnetic field immunity specifications (p. 7) since it is not 100% tested.

**ISB-DS-001-IL3022-A**  
**December 2016**

### Change

- Initial Release.

### **Datasheet Limitations**

The information and data provided in datasheets shall define the specification of the product as agreed between NVE and its customer, unless NVE and customer have explicitly agreed otherwise in writing. All specifications are based on NVE test protocols. In no event however, shall an agreement be valid in which the NVE product is deemed to offer functions and qualities beyond those described in the datasheet.

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### **Limiting Values**

Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the recommended operating conditions of the datasheet is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

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An ISO 9001 Certified Company

NVE Corporation  
11409 Valley View Road  
Eden Prairie, MN 55344-3617 USA  
Telephone: (952) 829-9217

[www.nve.com](http://www.nve.com)  
e-mail: [iso-info@nve.com](mailto:iso-info@nve.com)

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