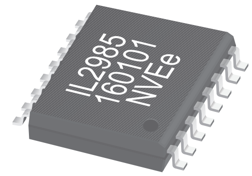
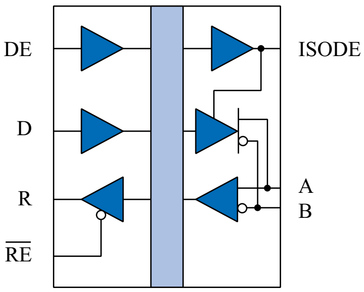


Low-Power 4 Mbps Isolated RS-485 Transceiver

Functional Diagram and Truth Table



IL2985

V_{ID} (A-B)	DE	$\overline{RE}$	R	D	Mode	Notes
≥ 200 mV	L	L	H	X	Receive	
≤–200mV	L	L	L	X		
Open	L	L	H	X		A/B failsafe
≥ 1.5 V	H	L	H	H	Drive	R reads back D information
≤–1.5 V	H	L	L	L		
≥ 1.5 V	H	H	Z	H		R tri-state (no output)
≤–1.5 V	H	H	Z	L		
X	L	H	Z	X	Disabled	R tri-state; A/B failsafe

Features

- Very low quiescent current (2.4 mA typ. I_{DD1Q} + I_{DD2Q})
- 4 Mbps data rate
- Supports up to 32 nodes
- 3 V to 5 V power supplies
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- 2500 V_{RMS} isolation voltage
- 44000 year barrier life
- 7 kV bus ESD protection
- Low EMC footprint
- Thermal shutdown protection
- –40°C to 85°C temperature range
- Meets or exceeds ANSI RS-485 and ISO 8482:1987(E)
- IEC 60747-17 (VDE 0884-17):2021-10 certified; UL 1577 recognized

Applications

- Metering
- Battery-powered RS-485 nodes
- Factory automation
- Industrial control networks
- Building environmental controls
- Equipment covered under IEC 61010-1 Edition 3

Description

The IL2985 is a low-power, galvanically isolated, high-speed differential bus transceiver. The device uses NVE's patented* low-power spintronic Tunneling Magnetoresistance (TMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The IL2985 delivers at least 1.5 V into a 54 Ω load for excellent data integrity over long cable lengths. The device is compatible with 5 V busses and 5 V or 3.3 V controller-side supplies.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs feature a "fail-safe if open" design, ensuring a logic high R-output if A/B are floating.

*U.S. Patent number 5,831,426; 6,300,617 and others.

REV. B

Absolute Maximum Ratings[8]

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55		150	°C	
Junction Temperature	T_J	–55		150	°C	
Voltage Range at A or B Bus Pins		–8		12.5	V	
Supply Voltage[1]	V_{DD1}, V_{DD2}	–0.5		7	V	
Digital Input Voltage		–0.5		V_{DD} + 0.5	V	
Digital Output Voltage		–0.5		V_{DD} + 1	V	
ESD (all bus nodes)		7			kV	HBM

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	V_{DD1} V_{DD2}	3.0 4.5		5.5 5.5	V	
Ambient Operating Temperature	T_A	–40		85	°C	
Junction Temperature	T_J	–40		100	°C	
Input Voltage at any Bus Terminal (separately or common mode)	V_I V_{IC}			12 –7	V	
High-Level Digital Input Voltage	V_{IH}	2.4 3.0		V_{DD1}	V	V_{DD1} = 3.3 V V_{DD1} = 5.0 V
Low-Level Digital Input Voltage	V_{IL}	0		0.8	V	
Differential Input Voltage[2]	V_{ID}			+12 / –7	V	
High-Level Output Current (Driver)	I_{OH}			60	mA	
High-Level Digital Output Current (Receiver)	I_{OH}			8	mA	
Low-Level Output Current (Driver)	I_{OL}	–60			mA	
Low-Level Digital Output Current (Receiver)	I_{OL}	–8			mA	
Digital Input Signal Rise and Fall Times	t_{IR}, t_{IF}	DC Stable				

Safety and Approvals

IEC 60747-17 (VDE 0884-17):2021-10 (Basic Isolation; VDE File Number 5016933-4880-0001)

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating: 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit.
- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180 °C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

UL 1577 (Component Recognition Program File Number E207481)

- 2500 V rating.
- Each part tested at 3000 V_{RMS} (4243 V_{PK}) for 1 second.
- Each lot sample tested at 2500 V_{RMS} (3536 V_{PK}) for 1 minute.

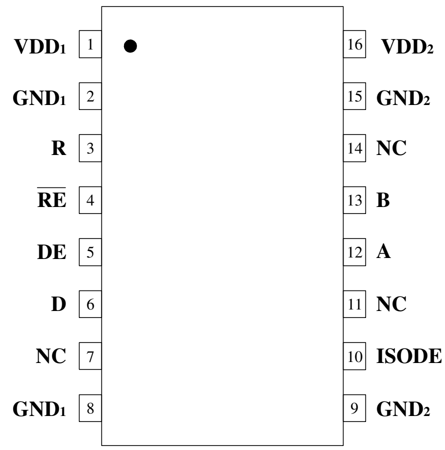
Soldering Profile

Per JEDEC J-STD-020C, MSL 1

NVE Corporation 11409 Valley View Road, Eden Prairie, MN 55344-3617 (952) 829-9217 www.nve.com YouTube.com/NveCorporation iso-apps@nve.com

Pin Connections

1	V_{DD1}	Input power supply
2	GND_1	Input power supply ground return (pin 2 is internally connected to pin 8)
3	R	Output data from bus
4	$\overline{RE}$	Read data enable (if $\overline{RE}$ is high, R= high impedance)
5	DE	Drive enable
6	D	Data input to bus
7	NC	No internal connection
8	GND_1	Input power supply ground return (pin 8 is internally connected to pin 2)
9	GND_2	Output power supply ground return (pin 9 is internally connected to pin 15)
10	ISODE	Isolated DE output for use in PROFIBUS applications where the state of the isolated drive enable node needs to be monitored.
11	NC	No internal connection
12	A	Non-inverting bus line
13	B	Inverting bus line
14	NC	No internal connection
15	GND_2	Output power supply ground return (pin 15 is internally connected to pin 9)
16	V_{DD2}	Output power supply



Driver Section

Electrical Specifications (T_{min} to T_{max} and V_{DD} = 4.5 V to 5.5 V unless otherwise stated)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Output voltage	V_O			V_{DD}	V	$I_O = 0$
Differential Output Voltage(2)	$\|V_{OD1}\|$			V_{DD}	V	$I_O = 0$
Differential Output Voltage(2)	V_{OD3}	1.5	2.3	5	V	R_L = 54 Ω, V_{DD} = 4.5 V
Change in Magnitude of Differential Output Voltage(3)	$\Delta\|V_{OD}\|$		±0.01	±0.2	V	R_L = 54 Ω or 100 Ω
Common Mode Output Voltage	V_{OC}			3	V	R_L = 54 Ω or 100 Ω
Change in Magnitude of Common Mode Output Voltage(3)	$\Delta\|V_{OC}\|$		±0.01	±0.2	V	R_L = 54 Ω or 100 Ω
Output Current	I_O			1 −0.8	mA	Output Disabled, V_O = 12 V_O = −7
High Level Input Current	I_{IH}			10	µA	V_I = 3.5 V
Low Level Input Current	I_{IL}			−10	µA	V_I = 0.4 V
Absolute |Short-circuit Output Current|	I_{OS}			250	mA	−7 V < V_O < 12 V
Quiescent Supply Current V_{DD1} = 5 V V_{DD1} = 3.3 V	I_{DD1Q}		0.65 0.4	0.8 0.7	mA	No Load; outputs enabled
Active Supply Current V_{DD1} = 5 V V_{DD1} = 3.3 V	I_{DD1}		2.3 1.2	3 1.6	mA	No Load; 4 Mbps data rate; outputs enabled

Receiver Section

Electrical Specifications (T_{min} to T_{max} and V_{DD} = 4.5 V to 5.5 V unless otherwise stated)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Positive-going Input Threshold Voltage	V_{IT+}			0.2	V	−7 V < V_{CM} < 12 V
Negative-going Input Threshold Voltage	V_{IT-}	−0.2			V	−7 V < V_{CM} < 12 V
Hysteresis Voltage ($V_{IT+} - V_{IT-}$)	V_{HYS}		70		mV	V_{CM} = 0 V, T = 25°C
High Level Digital Output Voltage	V_{OH}	V_{DD} − 0.2	V_{DD}		V	V_{ID} = 200 mV I_{OH} = −20 μA
Low Level Digital Output Voltage	V_{OL}			0.2	V	V_{ID} = −200 mV I_{OH} = 20 μA
High-impedance-state output current	I_{OZ}			±1	μA	V_O = 0.4 to (V_{DD2}−0.5) V
Line Input Current	I_I			1	mA	V_I = 12 V
				−0.8	mA	V_I = −7 V
Input Resistance	R_I	12			kΩ	
Quiescent Supply Current	I_{DD2Q}		1.75	1.9	mA	No load; outputs enabled
Active Supply Current	I_{DD2}		7.25	9	mA	No load; 4 Mbps data rate; outputs enabled

Switching Characteristics

V_{DD1} = 5 V, V_{DD2} = 5 V						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		4			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay(4)	t_{PD}		60	80	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Pulse Skew(5)	$t_{SK}(P)$		5	20	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Output Enable Time To High Level	t_{PZH}		60	80	ns	C_L = 15 pF
Output Enable Time To Low Level	t_{PZL}		60	80	ns	C_L = 15 pF
Output Disable Time From High Level	t_{PHZ}		60	80	ns	C_L = 15 pF
Output Disable Time From Low Level	t_{PLZ}		60	80	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$\|CM_H\|,\|CM_L\|$	30	50		kV/μs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns
V_{DD1} = 3.3 V, V_{DD2} = 5 V						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		4			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay(4)	t_{PD}		65	90	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Pulse Skew(5)	$t_{SK}(P)$		10	15	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Output Enable Time To High Level	t_{PZH}		65	90	ns	C_L = 15 pF
Output Enable Time To Low Level	t_{PZL}		65	90	ns	C_L = 15 pF
Output Disable Time From High Level	t_{PHZ}		65	90	ns	C_L = 15 pF
Output Disable Time From Low Level	t_{PLZ}		65	90	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$\|CM_H\|,\|CM_L\|$	30	50		kV/μs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns

Magnetic Field Immunity(7)

$V_{DD1} = 5$ V, $V_{DD2} = 5$ V						
Power Frequency Magnetic Immunity	H_{PF}		3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		4500		A/m	$t_p = 8\mu s$
Damped Oscillatory Magnetic Field	H_{OSC}		4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(8)	K_X		2.5			
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	$t_p = 8\mu s$
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(8)	K_X		2.5			

Insulation Specifications

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)			8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)			0.012	0.013		mm	
Barrier Resistance		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance		C_{IO}		7		pF	f = 1 MHz
Leakage Current				0.2		μA_{RMS}	240 V_{RMS}, 60 Hz
Comparative Tracking Index		CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
	DC		1500			V_{DC}	
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	θ_{JA}		67		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	θ_{JC}		12			
Junction–Ambient Thermal Resistance	θ_{JA}		46			2s2p PCB in free air per JESD51
Junction–Case (Top) Thermal Resistance	θ_{JC}		9			
Power Dissipation	P_D			1500	mW	

Notes:

1. All voltages are with respect to network ground except differential I/O bus voltages.
2. Differential input/output voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
3. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
4. Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
5. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel.
6. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
7. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 8.
8. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 8).

Supply Current vs. Speed

As shown in Figure 1, the IL2985 draws considerably less supply current than our standard isolated transceivers. The current increases slightly over the 4 Mbps operating range:

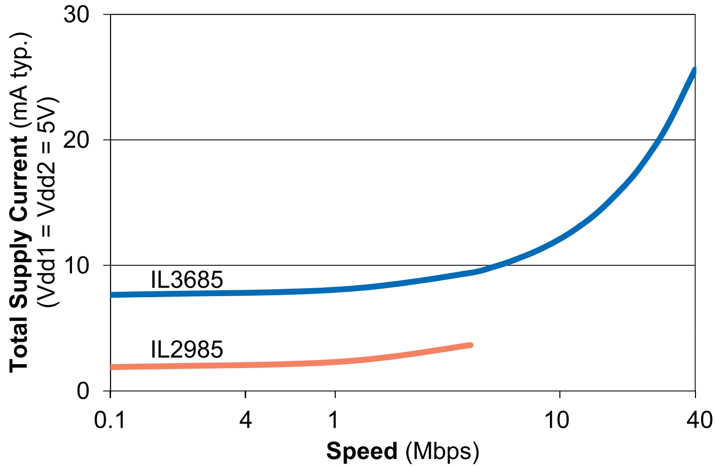


Figure 1. Supply current vs. speed.

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
Supply current vs. speed

Power Supply Decoupling

V_{DD1} and V_{DD2} should be bypassed with 0.1 µF typical (0.047 µF minimum) capacitors as close as possible to V_{DD} pins.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

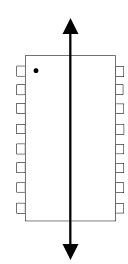
DC Correctness

The IL2985 incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power up, the bus outputs will follow the Function Table shown on Page 1. The DE input should be held low during power-up to eliminate false drive data pulses from the bus. An external power supply monitor to minimize glitches caused by slow power-up and power-down transients is not required.

Electromagnetic Compatibility

The IL2985 is fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. NVE conducted compliance tests in the categories below:

EN50081-1
  Residential, Commercial & Light Industrial
  Methods EN55022, EN55014
EN50082-2: Industrial Environment
  Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity)
ENV50204
  Radiated Field from Digital Telephones (Immunity Test)



Immunity to external magnetic fields is even higher if the field direction is "end-to-end" (rather than to "pin-to-pin") as shown above.

Application Information

Figure 2 shows typical connections to a bus and microcontroller, including typical termination and fail-safe resistors, and power supply decoupling capacitors:

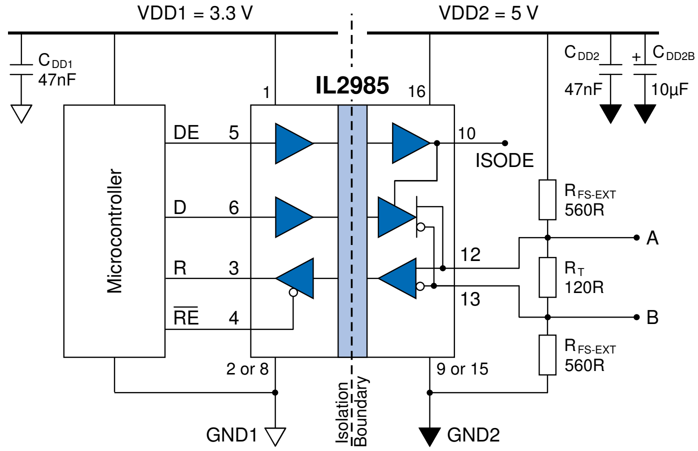


Figure 2. Typical connections.

Receiver Features
The receiver output “R” has tri-state capability via the active low $\overline{\text{RE}}$ input.

Driver Features
The RS-485 driver has a differential output and delivers at least 2.1 V across a 54 Ω load. Drivers feature low propagation delay skew to maximize bit width and minimize EMI. Drivers have tri-state capability via the active-high DE input.

Receiver Data Rate, Cables and Terminations
The IL2985 is intended for networks up to 4,000 feet (1,200 m), but the maximum data rate decreases as cable length increases. Twisted pair cable should be used in all networks since they tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receiver.

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RS-485 System with Isolated DC-DC Convertor

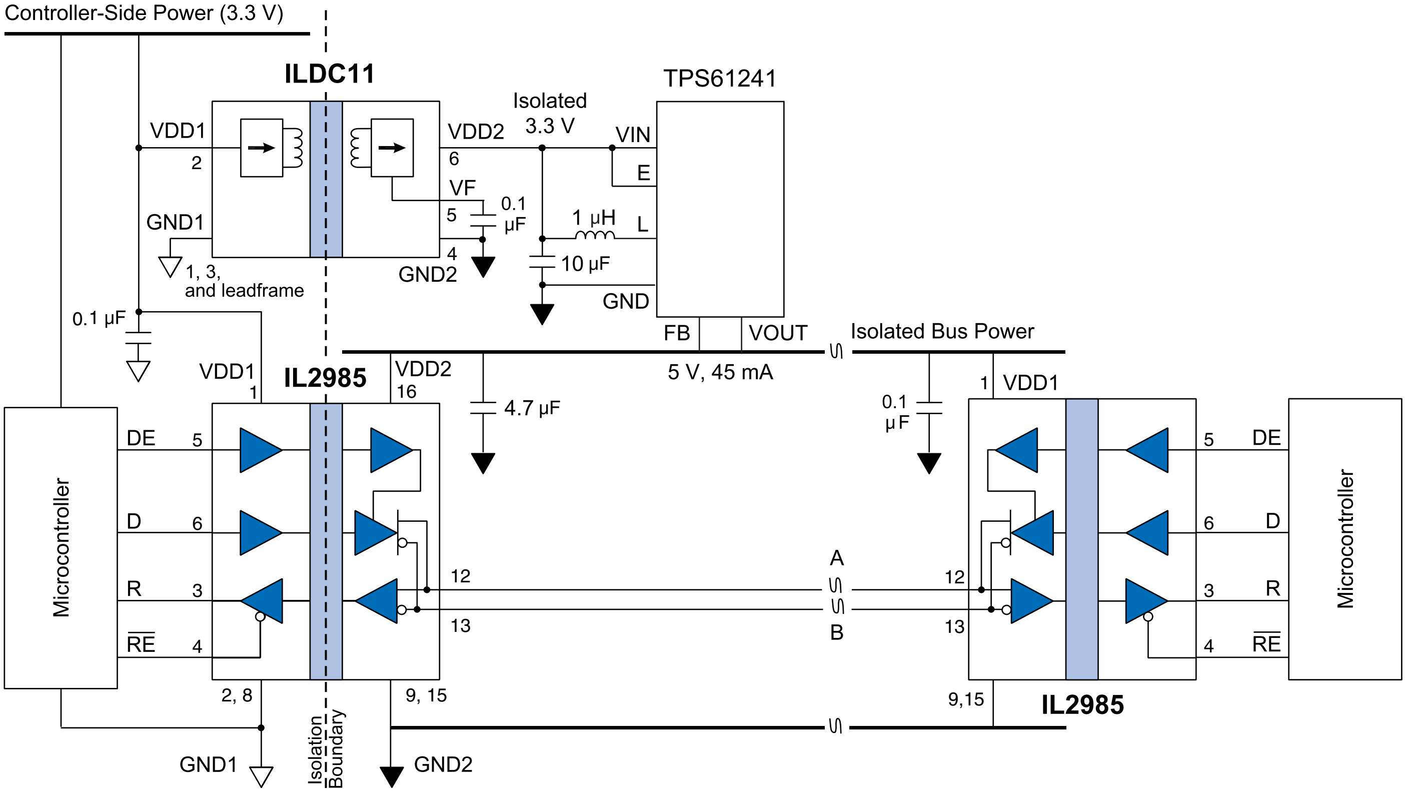


Figure 3. An RS-485 system with an ILDC11 isolated DC-DC convertor.

IL2985 transceivers are ideal for DC-DC convertor powered RS-485 systems because their bus-side quiescent supply current of less than 2 mA allows more nodes within the power budget. The NVE ILDC11 isolates the 3.3-volt controller supply, and an inexpensive boost regulator increases the supply to five volts. The isolated 5-volt capacity is 45 mA, which is enough to power a number of nodes without termination resistors.

Fail-Safe Operation

"Fail-safe operation" is defined here as the forcing of a logic high state on the "R" output in response to an open-circuit condition between the "A" and "B" lines of the bus, or when no drivers are active on the bus.

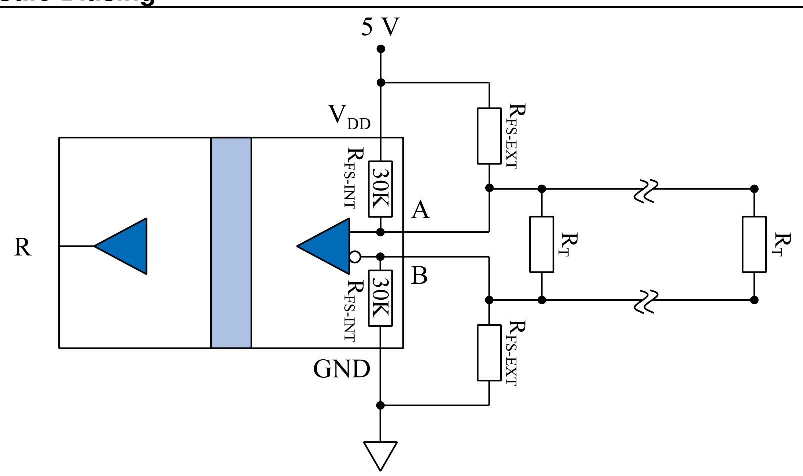
Proper biasing can ensure fail-safe operation, that is a known state when there are no active drivers on the bus. IL2985 Isolated Transceivers include internal pull-up and pull-down resistors of approximately 30 kΩ in the receiver section ($R_{FS\text{-}INT}$; see figure below). These internal resistors are designed to ensure failsafe operation but only if there are no termination resistors. The entire V_{DD} will appear between inputs "A" and "B" if there is no loading and no termination resistors, and there will be more than the required 200 mV with up to four RS-485 worst-case Unit Loads of 12 kΩ. Many designs operating below 1 Mbps or less than 1,000 feet are unterminated. Termination resistors may not be necessary for very low data rates and very short cable runs because reflections have time to settle before data sampling, which occurs at the middle of the bit interval.

In busses with low-impedance termination resistors however, the differential voltage across the conductor pair will be close to zero with no active drivers. In this case the state of the bus is indeterminate, and the idle bus will be susceptible to noise. For example, with 120 Ω termination resistors (R_T) on each end of the cable, and four Unit Loads (12 kΩ each), without external fail-safe biasing resistors the internal pull-up and pull-down resistors will produce a voltage between inputs "A" and "B" of only about 5 mV. This is not nearly enough to ensure a known state. External fail-safe biasing resistors ($R_{FS\text{-}EXT}$) at one end of the bus can ensure fail-safe operation with a terminated bus. Resistors should be selected so that under worst-case power supply and resistor tolerances there is at least 200 mV across the conductor pair with no active drivers to meet the input sensitivity specification of the RS-485 standard.

Using the same value for pull-up and pull-down biasing resistors maintains balance for positive- and negative going transitions. Lower-value resistors increase inactive noise immunity at the expense of quiescent power consumption. Note that each Unit Load on the bus adds a worst-case loading of 12 kΩ across the conductor pair, and 32 Unit Loads add 375 Ω worst-case loading. The more loads on the bus, the lower the required values of the biasing resistors.

In the example with two 120 Ω termination resistors and four Unit Loads, 560 Ω external biasing resistors provide more than 200 mV between "A" and "B" with adequate margin for power supply variations and resistor tolerances. This ensures a known state when there are no active drivers. Other illustrative examples are shown in the following table:

Fail-Safe Biasing

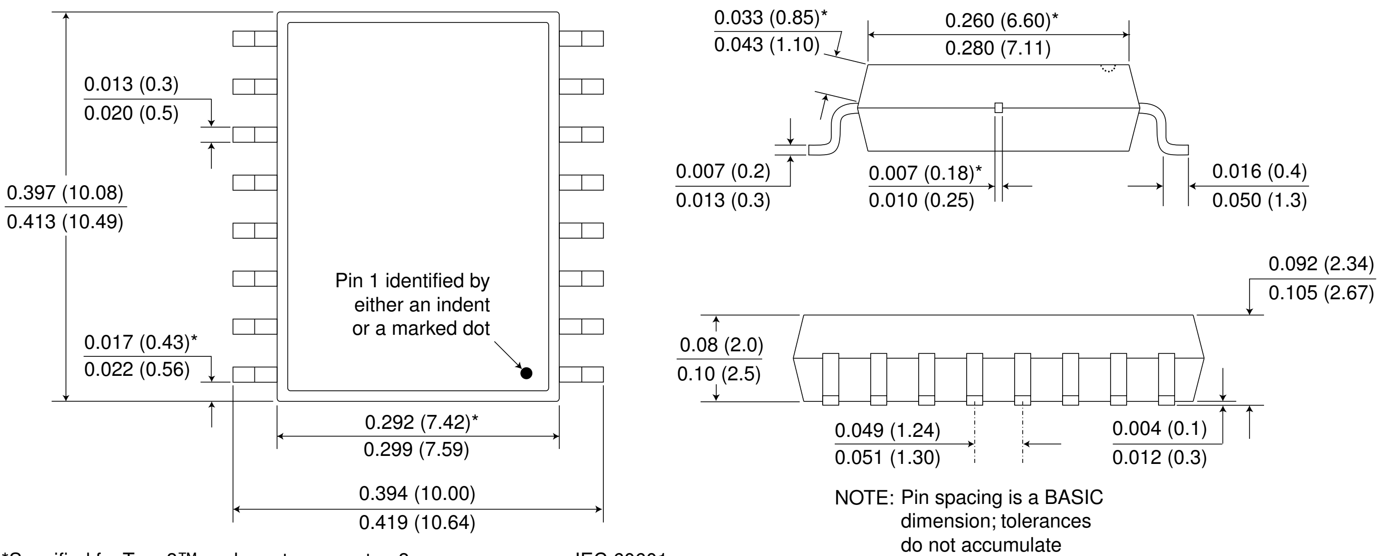


$R_{FS\text{-}EXT}$	R_T	Loading	Nominal $V_{A\text{-}B}$ (inactive)	Fail-Safe Operation?
Internal Only	None	Four unit loads (12 kΩ ea.)	238 mV	Yes
Internal Only	120 Ω	Four unit loads (12 kΩ ea.)	5 mV	No
560 Ω	120 Ω	Four unit loads (12 kΩ ea.)	254 mV	Yes
510 Ω	120 Ω	32 unit loads (12 kΩ ea.)	247 mV	Yes

Package Drawing

0.3" 16-pin SOIC Package

Dimensions in inches (mm); scale = approx. 5X

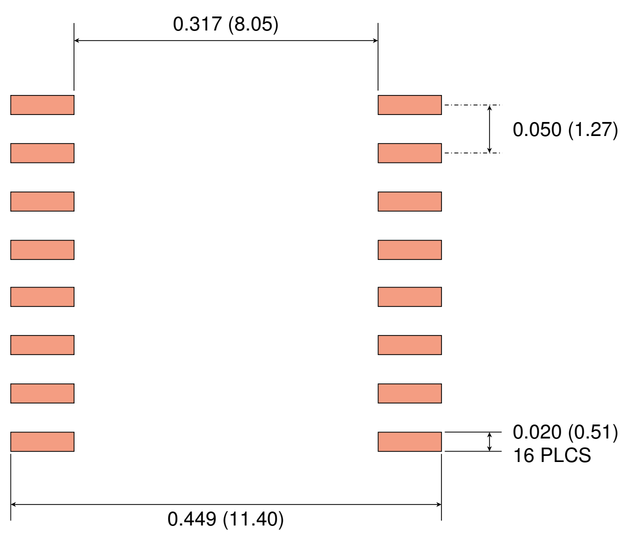


*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layout

0.3" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Ordering Information and Valid Part Numbers

IL 29 85 E TR13

Bulk Packaging
Blank = Tube
TR13 = 13" Tape and Reel

Package
E = RoHS Compliant 0.3" SOIC

Channel Configuration
85 = RS-485

Base Part Number
29 = Digital-In, Low-Power,
4 Mbps Transceiver

Product Family
IL = Isolators

Valid Part Numbers
IL2985E
IL2985E TR13

RoHS
COMPLIANT

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Revision History

ISB-DS-001-IL2985-REV-B
October 2022

Changes

- Clarified truth table (p. 1).
- IEC 60747-17 (VDE 0884-17):2021-10 certification (p. 3).
- Revised thermal specifications (p. 7).
- Delete minimum field immunity specifications (typical only) since they are not 100% tested.
- Added supply current vs. speed graph (p. 8).
- Added DC-DC convertor application circuit (Fig. 3; p. 10).

ISB-DS-001-IL2985-REV-A
June 2017

Change

- Initial release.

ISB-DS-001-IL2985-PRELIM3
May 2017

Change

- Updated speed, propagation delay, and supply current specifications based on more production lots.

ISB-DS-001-IL2985-PRELIM2
April 2017

Change

- Misc. updates.

ISB-DS-001-IL2985-PRELIM
June 2016

Change

- Preliminary Release.

Datasheet Limitations
The information and data provided in datasheets shall define the specification of the product as agreed between NVE and its customer, unless NVE and customer have explicitly agreed otherwise in writing. All specifications are based on NVE test protocols. In no event however, shall an agreement be valid in which the NVE product is deemed to offer functions and qualities beyond those described in the datasheet.

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