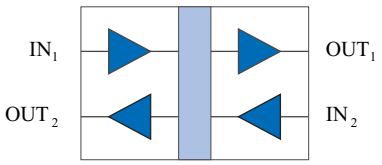
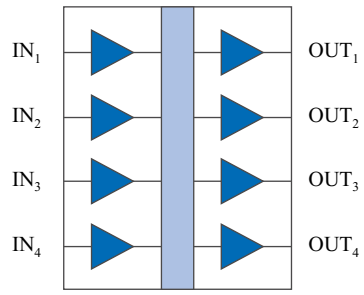
Low-Power Digital Isolators

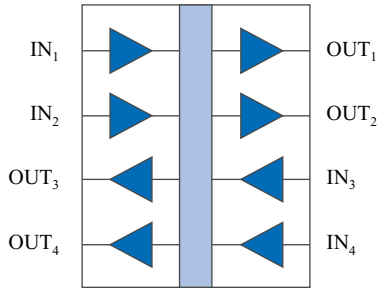
Functional Diagrams



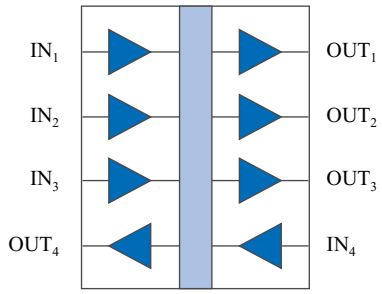
IL012



IL015



IL016



IL017

Features

- 0.3 mA/channel total typical quiescent current
- 10 Mbps guaranteed maximum data rate
- −40°C to +100°C
- No carriers or clocks for low EMI emissions
- 44000 year barrier life
- 50 kV/µs typical common mode transient immunity
- Excellent magnetic immunity
- VDE V 0884-11 certification and UL 1577 listing pending
- SOIC8 and wide-body 16-pin SOIC packages

Applications

- 4-20 mA loop-powered controls
- Battery-powered instruments
- SPI
- Multiplexed data transmission
- Ground loop elimination
- Logic level shifting

Description

NVE's IL01x low-power digital isolators use NVE's patented* spintronic Tunneling Magnetoresistance (TMR) technology for a remarkable combination of power efficiency and speed.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

Their unique design sensitive has no carriers or clocks, providing virtually undetectable EMI emissions.

Parts are available in various two-channel and four-channel configurations.

PRELIM.

Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	−55		150	°C	
Junction Temperature	T_J	−55		150	°C	
Ambient Operating Temperature[1]	T_A	−40		100	°C	
Supply Voltage	V_{DD1}, V_{DD2}	−0.5		7	V	
Input Voltage	V_I	−0.5		V_{DD}+0.5	V	
Output Voltage	V_O	−0.5		V_{DD}+0.5	V	
Output Current Drive	I_O			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	T_A	−40		100	°C	
Junction Temperature	T_J	−40		110	°C	
Supply Voltage	V_{DD1}, V_{DD2}	3		5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	µs	

Insulation Specifications

Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)							
SOIC8			4.03			mm	
SOIC16			8.03	8.3			Per IEC 60601
Total Barrier Thickness (internal)			0.012	0.016		mm	
Leakage Current[5]				0.2		µA	240 V_{RMS}, 60 Hz
Barrier Resistance[5]				$>10^{14}$		Ω	500 V
Barrier Capacitance[5]				4		pF	f = 1 MHz
Comparative Tracking Index		CTI	≥600			V_{RMS}	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
	DC		1500			V_{DC}	
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	SOIC8 SOIC16	θ_{JA}		60 60		°C/W	Soldered to double-sided board; free air
Junction–Case (Top) Thermal Resistance	SOIC8 SOIC16	θ_{JT}		10 20		°C/W	
Power Dissipation	SOIC8 SOIC16	P_D			675 800	mW	

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Safety and Approvals

VDE V 0884-11 (Basic Isolation; approval pending under VDE File Number 5016933-4880-0001)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}) 4000 V_{PK}
- Surge rating 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180°C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)
Reinforced Insulation; Pollution Degree II; Material Group III
300 V_{RMS} Working Voltage

UL 1577 (pending under Component Recognition Program File Number E207481)
Tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

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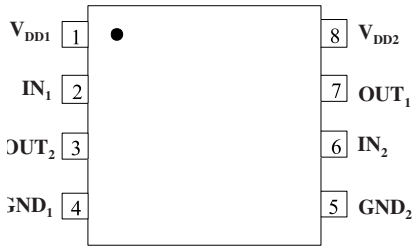
IL012-3 Pin Connections

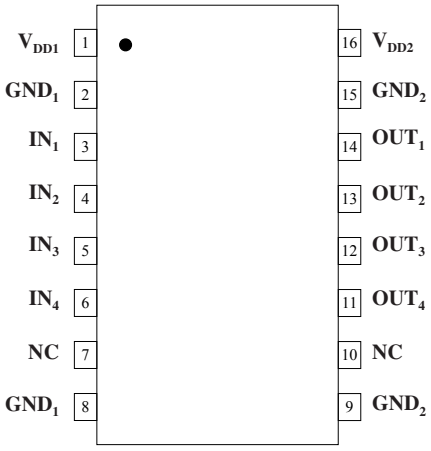
1	V_{DD1}	Supply voltage
2	IN_1	Data in, channel 1
3	OUT_2	Data out, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	IN_2	Data in, channel 2
7	OUT_1	Data out, channel 1
8	V_{DD2}	Supply voltage



IL012-3

IL015 Pin Connections

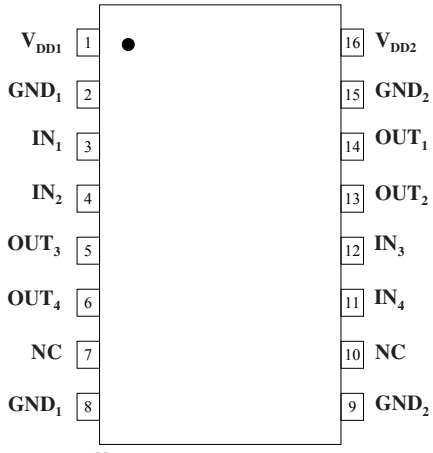
1	V_{DD1}	Supply voltage
2	GND_1	Ground return for V_{DD1}*
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	IN_3	Data in, channel 3
6	IN_4	Data in, channel 4
7	NC	No connection
8	GND_1	Ground return for V_{DD1}*
9	GND_2	Ground return for V_{DD2}*
10	NC	No connection
11	OUT_4	Data out, channel 4
12	OUT_3	Data out, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2}*
16	V_{DD2}	Supply voltage



IL015

IL016 Pin Connections

1	V_{DD1}	Supply voltage
2	GND_1	Ground Return for V_{DD1}*
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	OUT_3	Data out, channel 3
6	OUT_4	Data out, channel 4
7	NC	No connection
8	GND_1	Ground Return for V_{DD1}*
9	GND_2	Ground Return for V_{DD2}*
10	NC	No connection
11	IN_4	Data in, channel 4
12	IN_3	Data in, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground Return for V_{DD2}*
16	V_{DD2}	Supply voltage

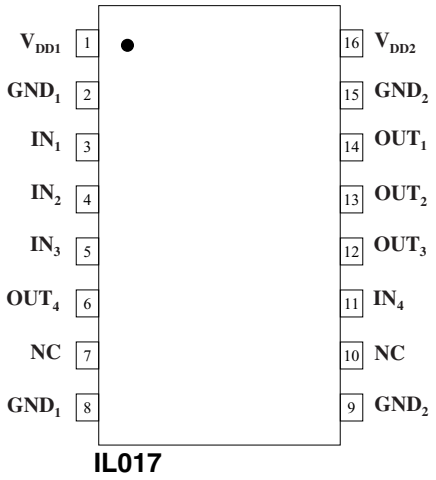


IL016

***NOTE:** Pins 2 and 8 are internally connected, as are pins 9 and 15.

IL017 Pin Connections

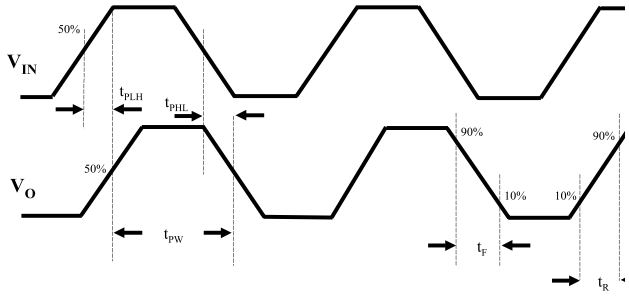
1	V_{DD1}	Supply voltage
2	GND_1	Ground return for V_{DD1}*
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	IN_3	Data in, channel 3
6	OUT_4	Data out, channel 4
7	NC	No connection
8	GND_1	Ground return for V_{DD1}*
9	GND_2	Ground return for V_{DD2}*
10	NC	No connection
11	IN_4	Data in, channel 4
12	OUT_3	Data out, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2}*
16	V_{DD2}	Supply voltage



IL017

***NOTE:** Pins 2 and 8 are internally connected, as are pins 9 and 15.

Timing Diagram



Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_R	Rise Time
t_F	Fall Time

3.3 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
V_{DD1} Quiescent Supply Current						
IL012	I_{DD1}		0.3	0.5	mA	
IL015			8	15	µA	
IL016			0.6	1.0	mA	
IL017			0.3	0.5	mA	
V_{DD2} Quiescent Supply Current						
IL012	I_{DD2}		0.3	0.5	mA	
IL015			1.2	2.0	mA	
IL016			0.6	1.0	mA	
IL017			0.9	1.5	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} − 0.1	V_{DD}		V	I_O = −20 µA, V_I = V_{IH}
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.5	0.8		I_O = 4 mA, V_I = V_{IL}

Switching Specifications (V_{DD} = 3.3 V)						
Maximum Data Rate		10			Mbps	C_L = 15 pF
Pulse Width[7]	PW	50			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		30	60	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		30	60	ns	C_L = 15 pF
Pulse Width Distortion [2]	PWD		10	18	ns	C_L = 15 pF
Propagation Delay Skew [3]	t_{PSK}		10	18	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		2	4	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		2	4	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	$\|CM_H\|$,$\|CM_L\|$	30	50		kV/µs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns
Channel-to-Channel Skew	t_{CSK}		15	25	ns	C_L = 15 pF
Dynamic Power Consumption[6]			140	240	µA/Mbps	per channel

Magnetic Field Immunity[8] (V_{DD1} = V_{DD2} = 3.3V)						
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50 Hz / 60 Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	t_p = 8 µs
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1 Hz – 1 MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

5 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
V_{DD1} Quiescent Supply Current						
IL012	I_{DD1}		0.5	0.75	mA	
IL015			10	20	µA	
IL016			1	1.5	mA	
IL017			0.5	0.75	mA	
V_{DD2} Quiescent Supply Current						
IL012	I_{DD2}		0.5	0.75	mA	
IL015			2	3	mA	
IL016			1	1.5	mA	
IL017			1.5	2.25	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} − 0.1	V_{DD}		V	I_O = −20 µA, V_I = V_{IH}
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.5	0.8		I_O = 4 mA, V_I = V_{IL}

Switching Specifications (V_{DD} = 5V)						
Maximum Data Rate		10			Mbps	C_L = 15 pF
Pulse Width[7]	PW	50			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		20	40	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		20	40	ns	C_L = 15 pF
Pulse Width Distortion[2]	PWD		8	15	ns	C_L = 15 pF
Propagation Delay Skew[3]	t_{PSK}		8	15	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		2	4	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		2	4	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	$\|CM_H\|$,$\|CM_L\|$	30	50		kV/µs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns
Channel-to-Channel Skew	t_{CSK}		10	15	ns	C_L = 15 pF
Dynamic Power Consumption[6]			200	340	µA/Mbps	per channel

Magnetic Field Immunity[8] (V_{DD1} = V_{DD2} = 5V)						
Power Frequency Magnetic Immunity	H_{PF}		3500		A/m	50 Hz / 60 Hz
Pulse Magnetic Field Immunity	H_{PM}		4500		A/m	t_p = 8 µs
Damped Oscillatory Magnetic Field	H_{OSC}		4500		A/m	0.1 Hz – 1 MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
6. Dynamic power consumption is calculated per channel and is supplied by the channel's input-side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 7.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 7).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

Application Information

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

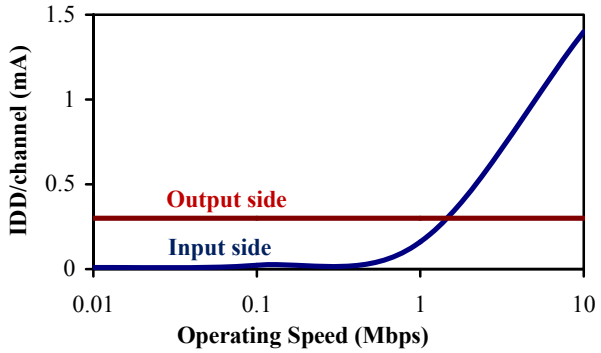
These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

EN50081-1
Residential, Commercial & Light Industrial
Methods EN55022, EN55014
EN50082-2: Industrial Environment
Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)
ENV50204
Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin."

Dynamic Power Consumption

IsoLoop Isolators achieve their low EMI emissions and low power consumption from a unique edge-triggered architecture. Most of the power is consumed on the output side, which is not dependant on operating frequency. Input side power consumption is generally lower, but has some dependence on operating frequency. Typical power consumption is shown in the following graph:



Typical supply current per channel, VDD = 3.3 V; 25°C.

Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR 47 nF ceramic capacitors. Capacitors must be located as close as possible to the V_{DD} pins.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

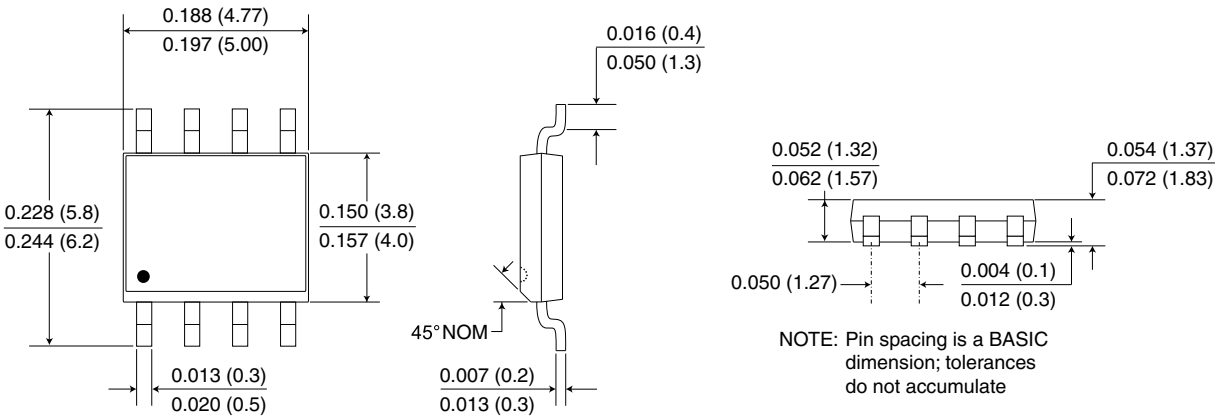
Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

Package Drawings

8-pin SOIC8 Package (IL012-3)

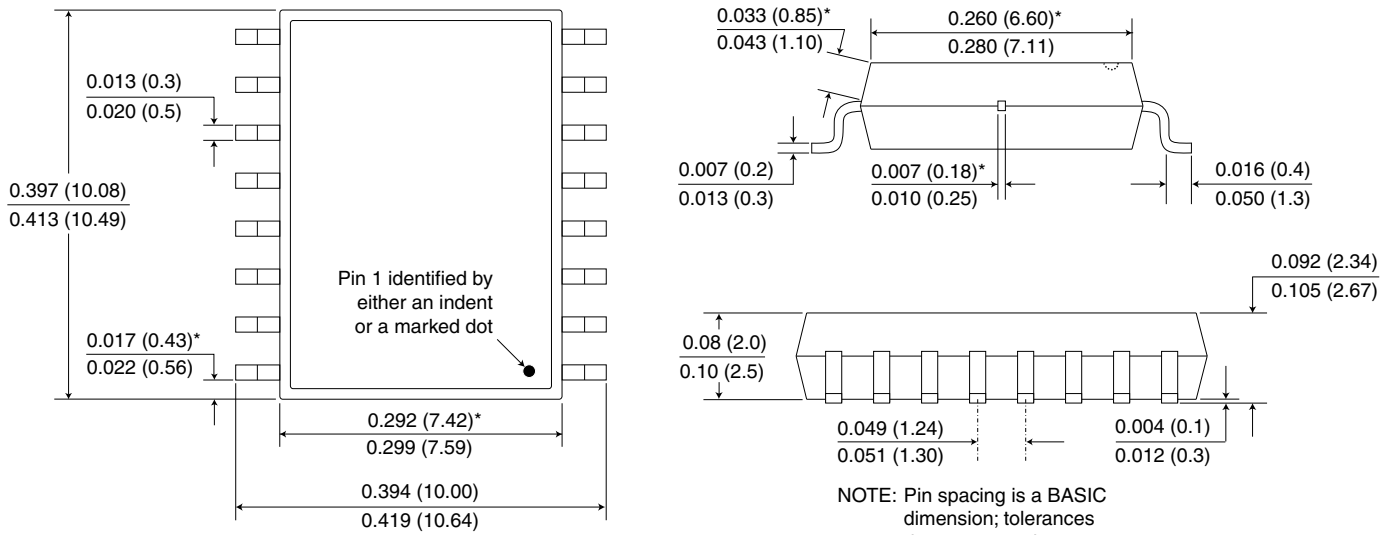
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

16-pin 0.3" SOIC16 Package (IL015 / IL016 / IL017)

Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

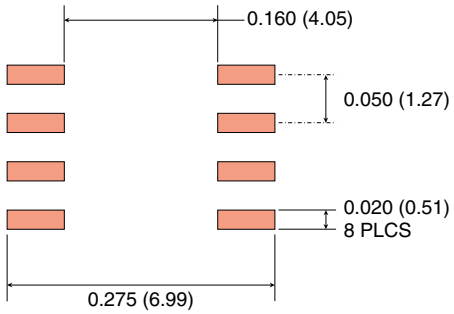
*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

RoHS COMPLIANT

Recommended Pad Layouts

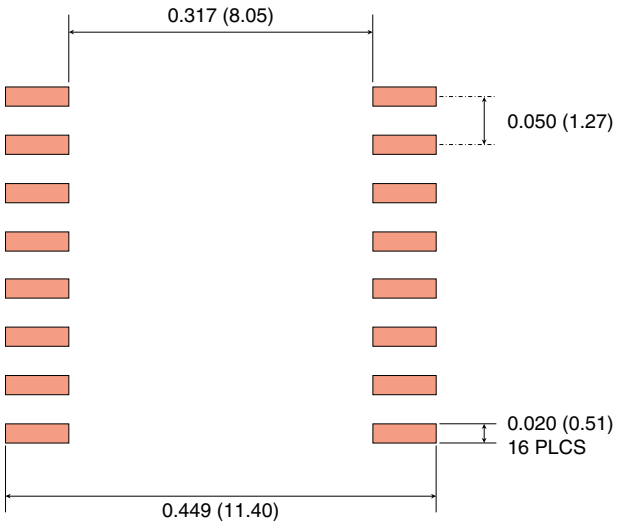
SOIC8 Pad Layout

Dimensions in inches (mm); scale = approx. 5X



SOIC16 Pad Layout

Dimensions in inches (mm); scale = approx. 5X



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Ordering Information

IL 0 17 E TR13

Bulk Packaging
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Package
E = 0.3" SOIC16 (RoHS)
-3E = 0.15" SOIC8 (RoHS)

Channel Configuration
12 = 1 Transmit Channel
1 Receive Channel
0.15" SOIC8

15 = 4 Transmit Channels
0.3" SOIC16

16 = 2 Transmit Channels
2 Receive Channels
0.3" SOIC16

17 = 3 Transmit Channels
1 Receive Channel
0.3" SOIC16

Base Part Number
0 = Low Power

Product Family
IL = Isolators

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ISB-DS-001-IL01x-PRELIM
March 2018

Changes

- Preliminary Release.

Datasheet Limitations
The information and data provided in datasheets shall define the specification of the product as agreed between NVE and its customer, unless NVE and customer have explicitly agreed otherwise in writing. All specifications are based on NVE test protocols. In no event however, shall an agreement be valid in which the NVE product is deemed to offer functions and qualities beyond those described in the datasheet.

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