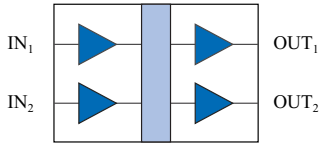
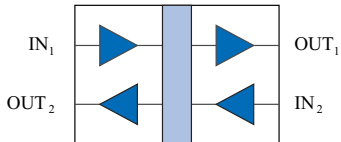


## Low-Power Digital Isolators

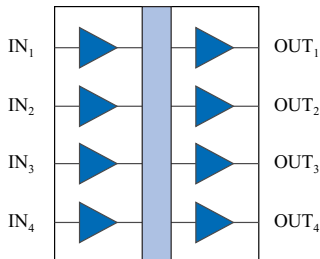
### Functional Diagrams



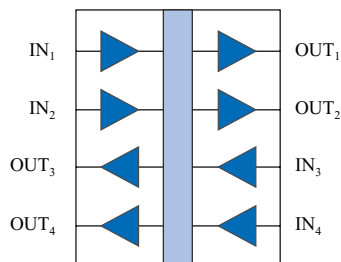
**IL011**



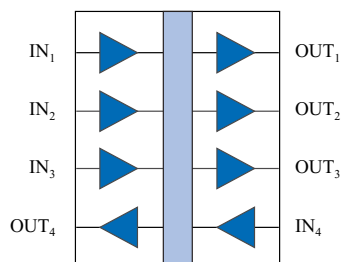
**IL012**



**IL015**



**IL016**



**IL017**

### Features

- 0.3 mA/channel total typical quiescent current
- 10 Mbps guaranteed maximum data rate
- Extended 2.5 to 5.5 volt supply range
- -40 °C to +100 °C
- No carriers or clocks for low EMI emissions
- 44000 year barrier life
- 50 kV/μs typical common mode transient immunity
- Excellent magnetic immunity
- VDE V 0884-11 / IEC 60747-17 certified; UL 1577 listed
- SOIC8 and wide-body 16-pin SOIC packages

### Applications

- 4-to-20 mA loop-powered controls
- Battery-powered instruments
- SPI
- Multiplexed data transmission
- Ground loop elimination
- Logic level shifting

### Description

NVE's IL01x low-power digital isolators use NVE's patented\* spintronic Tunneling Magnetoresistance (TMR) technology for a remarkable combination of power efficiency and speed.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

Their unique design sensitive has no carriers or clocks, providing virtually undetectable EMI emissions.

Parts are available in various two-channel and four-channel configurations.

## Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	$T_S$	-55		150	°C	
Junction Temperature	$T_J$	-55		150	°C	
Ambient Operating Temperature <sup>(1)</sup>	$T_A$	-40		100	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	-0.5		7	V	
Input Voltage	$V_I$	-0.5		$V_{DD}+0.5$	V	
Output Voltage	$V_O$	-0.5		$V_{DD}+0.5$	V	
Output Current Drive	$I_O$			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

## Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	$T_A$	-40		100	°C	
Junction Temperature	$T_J$	-40		110	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	2.5		5.5	V	
Logic High Input Voltage	$V_{IH}$	2.4		$V_{DD}$	V	
Logic Low Input Voltage	$V_{IL}$	0		0.8	V	
Input Signal Rise and Fall Times	$t_{IR}, t_{IF}$			1	μs	

## Safety and Approvals

**VDE V 0884-11 / IEC 60747-17** (Basic Isolation; VDE File Number 5016933-4880-0001)

- Isolation voltage ( $V_{ISO}$ ) 2500  $V_{RMS}$ .
- Transient overvoltage ( $V_{IOTM}$ ) 4000  $V_{PK}$ .
- Surge rating 4000 V.
- Each part tested at 1590  $V_{PK}$  for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000  $V_{PK}$  for 60 sec.; then 1358  $V_{PK}$  for 10 sec. with 5 pC partial discharge limit.
- Working Voltage ( $V_{IORM}$ ; pollution degree 2):

Package	Part No. Suffix	Working Voltage
SOIC8	-3	400 $V_{RMS}$
Wide-body SOIC16/ True 8™	None	500 $V_{RMS}$

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	$T_S$	180	°C
Safety rating power (180°C)	$P_S$	270	mW
Supply current safety rating (total of supplies)	$I_S$	54	mA

**UL 1577** (pending under Component Recognition Program File Number E207481)

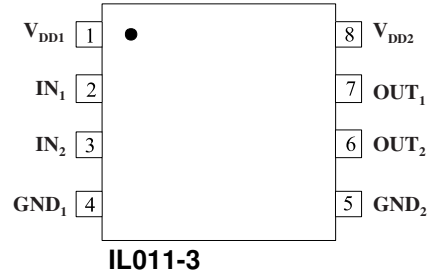
Tested at 3000  $V_{RMS}$  (4240  $V_{PK}$ ) for 1 second; each lot sample tested at 2500  $V_{RMS}$  (3530  $V_{PK}$ ) for 1 minute

## Soldering Profile

Per JEDEC J-STD-020C, MSL 1

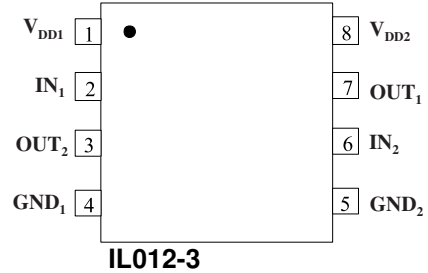
### IL011-3 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	IN <sub>1</sub>	Data in, channel 1
3	IN <sub>2</sub>	Data in, channel 2
4	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
5	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
6	OUT <sub>2</sub>	Data out, channel 2
7	OUT <sub>1</sub>	Data out, channel 1
8	V <sub>DD2</sub>	Supply voltage



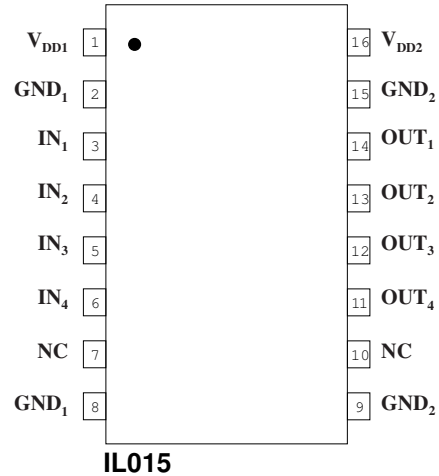
### IL012-3 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	IN <sub>1</sub>	Data in, channel 1
3	OUT <sub>2</sub>	Data out, channel 2
4	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
5	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
6	IN <sub>2</sub>	Data in, channel 2
7	OUT <sub>1</sub>	Data out, channel 1
8	V <sub>DD2</sub>	Supply voltage



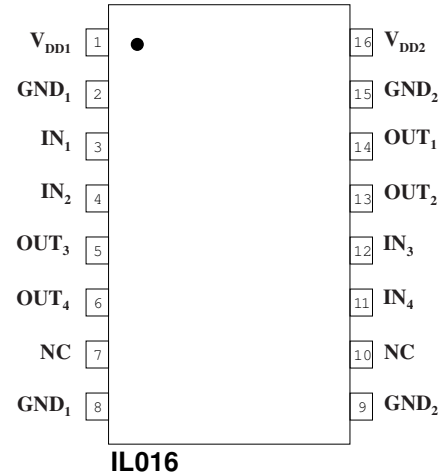
## IL015 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> *
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	IN <sub>3</sub>	Data in, channel 3
6	IN <sub>4</sub>	Data in, channel 4
7	NC	No connection
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> *
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> *
10	NC	No connection
11	OUT <sub>4</sub>	Data out, channel 4
12	OUT <sub>3</sub>	Data out, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> *
16	V <sub>DD2</sub>	Supply voltage



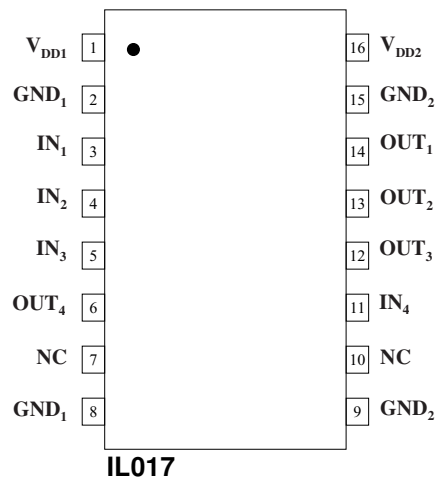
## IL016 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground Return for V <sub>DD1</sub> *
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	OUT <sub>3</sub>	Data out, channel 3
6	OUT <sub>4</sub>	Data out, channel 4
7	NC	No connection
8	GND <sub>1</sub>	Ground Return for V <sub>DD1</sub> *
9	GND <sub>2</sub>	Ground Return for V <sub>DD2</sub> *
10	NC	No connection
11	IN <sub>4</sub>	Data in, channel 4
12	IN <sub>3</sub>	Data in, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground Return for V <sub>DD2</sub> *
16	V <sub>DD2</sub>	Supply voltage



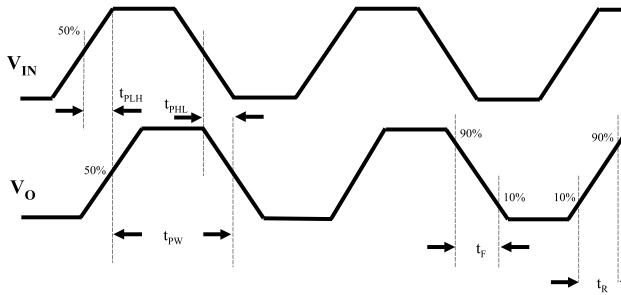
## IL017 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> *
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	IN <sub>3</sub>	Data in, channel 3
6	OUT <sub>4</sub>	Data out, channel 4
7	NC	No connection
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> *
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> *
10	NC	No connection
11	IN <sub>4</sub>	Data in, channel 4
12	OUT <sub>3</sub>	Data out, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> *
16	V <sub>DD2</sub>	Supply voltage



\*NOTE: Pins 2 and 8 are internally connected, as are pins 9 and 15.

**Timing Diagram**



**Legend**

$t_{PLH}$	Propagation Delay, Low to High
$t_{PHL}$	Propagation Delay, High to Low
$t_{PW}$	Minimum Pulse Width
$t_R$	Rise Time
$t_F$	Fall Time

3.3 Volt Electrical Specifications ( $T_{min}$ to $T_{max}$ unless otherwise stated)						
Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
$V_{DD1}$ Quiescent Supply Current						
IL011	$I_{DD1}$		8	15	$\mu\text{A}$	
IL012			0.3	0.5	$\text{mA}$	
IL015			10	15	$\mu\text{A}$	
IL016			0.4	1.0	$\text{mA}$	
IL017			0.3	0.5	$\text{mA}$	
$V_{DD2}$ Quiescent Supply Current						
IL011	$I_{DD2}$		0.6	1.0	$\text{mA}$	
IL012			0.3	0.5	$\text{mA}$	
IL015			1.2	2.0	$\text{mA}$	
IL016			0.4	1.0	$\text{mA}$	
IL017			0.9	1.5	$\text{mA}$	
Logic Input Current	$I_I$	-10		10	$\mu\text{A}$	
Logic High Output Voltage	$V_{OH}$	$V_{DD} - 0.1$	$V_{DD}$		V	$I_O = -20 \mu\text{A}, V_I = V_{IH}$
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			$I_O = -4 \text{mA}, V_I = V_{IH}$
Logic Low Output Voltage	$V_{OL}$		0	0.1	V	$I_O = 20 \mu\text{A}, V_I = V_{IL}$
				0.5		0.8

Magnetic Field Immunity <sup>(8)</sup> ( $V_{DD1} = V_{DD2} = 3.3\text{V}$ )						
Power Frequency Magnetic Immunity	$H_{PF}$		1500		A/m	50 Hz / 60 Hz
Pulse Magnetic Field Immunity	$H_{PM}$		2000		A/m	$t_p = 8 \mu\text{s}$
Damped Oscillatory Magnetic Field	$H_{OSC}$		2000		A/m	0.1 Hz – 1 MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	$K_X$		2.5			

5 Volt Electrical Specifications ( $T_{min}$ to $T_{max}$ unless otherwise stated)						
Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
$V_{DD1}$ Quiescent Supply Current						
IL011	$I_{DD1}$		10	20	$\mu\text{A}$	
IL012			0.5	0.75	$\text{mA}$	
IL015			17	25	$\mu\text{A}$	
IL016			0.7	1.5	$\text{mA}$	
IL017			0.5	0.75	$\text{mA}$	
$V_{DD2}$ Quiescent Supply Current						
IL011	$I_{DD2}$		1	1.5	$\text{mA}$	
IL012			0.5	0.75	$\text{mA}$	
IL015			2	3	$\text{mA}$	
IL016			0.7	1.5	$\text{mA}$	
IL017			1.5	2.25	$\text{mA}$	
Logic Input Current	$I_I$	-10		10	$\mu\text{A}$	
Logic High Output Voltage	$V_{OH}$	$V_{DD} - 0.1$	$V_{DD}$		V	$I_O = -20 \mu\text{A}, V_I = V_{IH}$
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			$I_O = -4 \text{mA}, V_I = V_{IH}$
Logic Low Output Voltage	$V_{OL}$		0	0.1	V	$I_O = 20 \mu\text{A}, V_I = V_{IL}$
				0.5		0.8

Magnetic Field Immunity <sup>(8)</sup> ( $V_{DD1} = V_{DD2} = 5\text{V}$ )						
Power Frequency Magnetic Immunity	$H_{PF}$		3500		A/m	50 Hz / 60 Hz
Pulse Magnetic Field Immunity	$H_{PM}$		4500		A/m	$t_p = 8 \mu\text{s}$
Damped Oscillatory Magnetic Field	$H_{OSC}$		4500		A/m	0.1 Hz – 1 MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	$K_X$		2.5			

Switching Specifications ( $3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )						
Maximum Data Rate		10			Mbps	$C_L = 15\text{ pF}$
Pulse Width <sup>(7)</sup>	PW	50			ns	50% Points, $V_O$
Propagation Delay Input to Output (High to Low)	$t_{PHL}$		50	100	ns	$C_L = 15\text{ pF}$
Propagation Delay Input to Output (Low to High)	$t_{PLH}$		50	100	ns	$C_L = 15\text{ pF}$
Pulse Width Distortion <sup>(2)</sup>	PWD		25	50	ns	$C_L = 15\text{ pF}$
Propagation Delay Skew <sup>(3)</sup>	$t_{PSK}$		25	50	ns	$C_L = 15\text{ pF}$
Output Rise Time (10%–90%)	$t_R$		2	4	ns	$C_L = 15\text{ pF}$
Output Fall Time (10%–90%)	$t_F$		2	4	ns	$C_L = 15\text{ pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	$ CM_H ,  CM_L $	30	50		kV/ $\mu\text{s}$	$V_{CM} = 1500\text{ V}_{DC}$ $t_{TRANSIENT} = 25\text{ ns}$
Channel-to-Channel Skew	$t_{CSK}$		10	15	ns	$C_L = 15\text{ pF}$
Dynamic Power Consumption <sup>(6)</sup>			200	340	$\mu\text{A}/\text{Mbps}$	per channel

Insulation Specifications						
Creepage Distance (external)						
SOIC8		4.03			mm	Per IEC 60601
SOIC16		8.03	8.3			
Total Barrier Thickness (internal)		0.012	0.016		mm	
Leakage Current <sup>(5)</sup>			0.2		$\mu\text{A}$	240 $V_{RMS}$ , 60 Hz
Barrier Resistance <sup>(5)</sup>			$>10^{14}$		$\Omega$	500 V
Barrier Capacitance <sup>(5)</sup>			4		pF	$f = 1\text{ MHz}$
Comparative Tracking Index	CTI	$\geq 600$			$V_{RMS}$	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	$V_{IO}$	1000		$V_{RMS}$	At maximum operating temperature
	DC		1500		$V_{DC}$	
Barrier Life			44000		Years	100°C, 1000 $V_{RMS}$ , 60% CL activation energy

Thermal Characteristics							
Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	SOIC8	$\theta_{JA}$		134			Double-sided PCB in free air
	0.3" SOIC16			67			
Junction–Case (Top) Thermal Resistance	SOIC8	$\theta_{JC}$		10		$^{\circ}\text{C}/\text{W}$	
	0.3" SOIC16			12			
Junction–Ambient Thermal Resistance	0.3" SOIC	$\theta_{JA}$		46		2s2p PCB in free air per JESD51	
Junction–Case (Top) Thermal Resistance		$\theta_{JC}$		9			
Power Dissipation	SOIC8 0.3" SOIC16	$P_D$			675 1500	mW	

### Notes:

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as  $t_{PHL} - t_{PLH}$ . %PWD is equal to PWD divided by pulse width.
3.  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  between devices at 25°C.
4.  $CM_H$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common mode input voltage that can be sustained while maintaining  $V_O < 0.8\text{ V}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
6. Dynamic power consumption is calculated per channel and is supplied by the channel's input-side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 9.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 9).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.



## Application Information

### Electrostatic Discharge Sensitivity

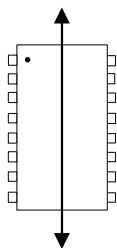
This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

### Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

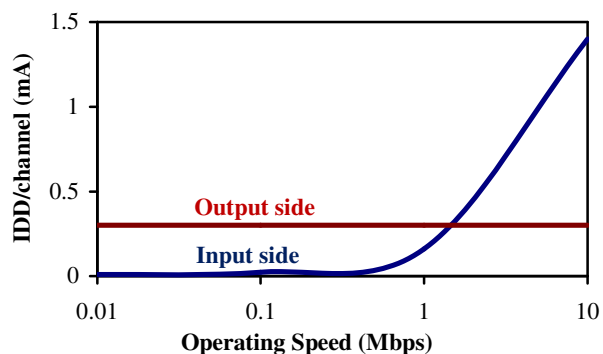
These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown below:



### Dynamic Power Consumption

IsoLoop Isolators achieve their low EMI emissions and low power consumption from a unique edge-triggered architecture. Most of the power is consumed on the output side, which is not dependant on operating frequency. Input side power consumption is generally lower, but has some dependence on operating frequency. Typical power consumption is shown in the following graph:



Typical supply current per channel, VDD = 3.3 V; 25°C.

### Power Supply Decoupling

Both power supplies should be decoupled with 0.1  $\mu$ F typical (0.047  $\mu$ F minimum) capacitors as close as possible to the V<sub>DD</sub> pins.

### Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

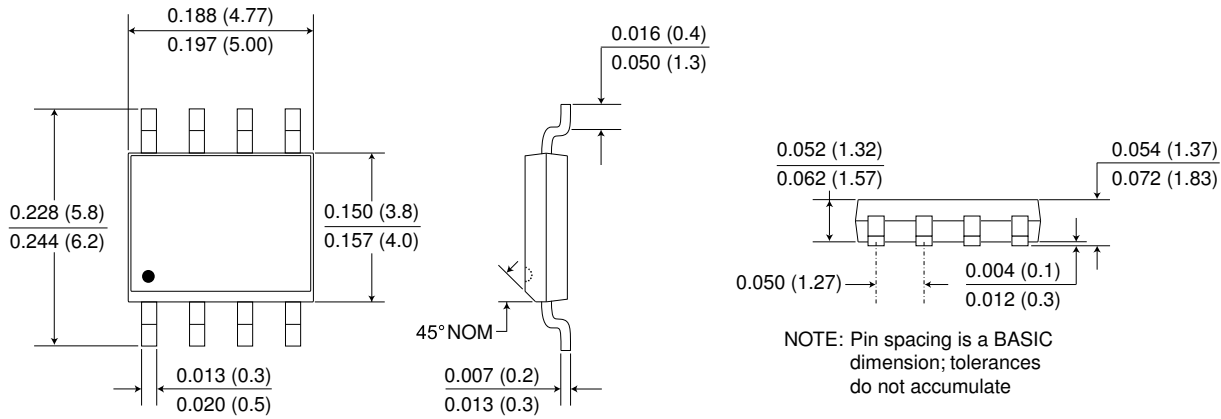
### Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

**Package Drawings**

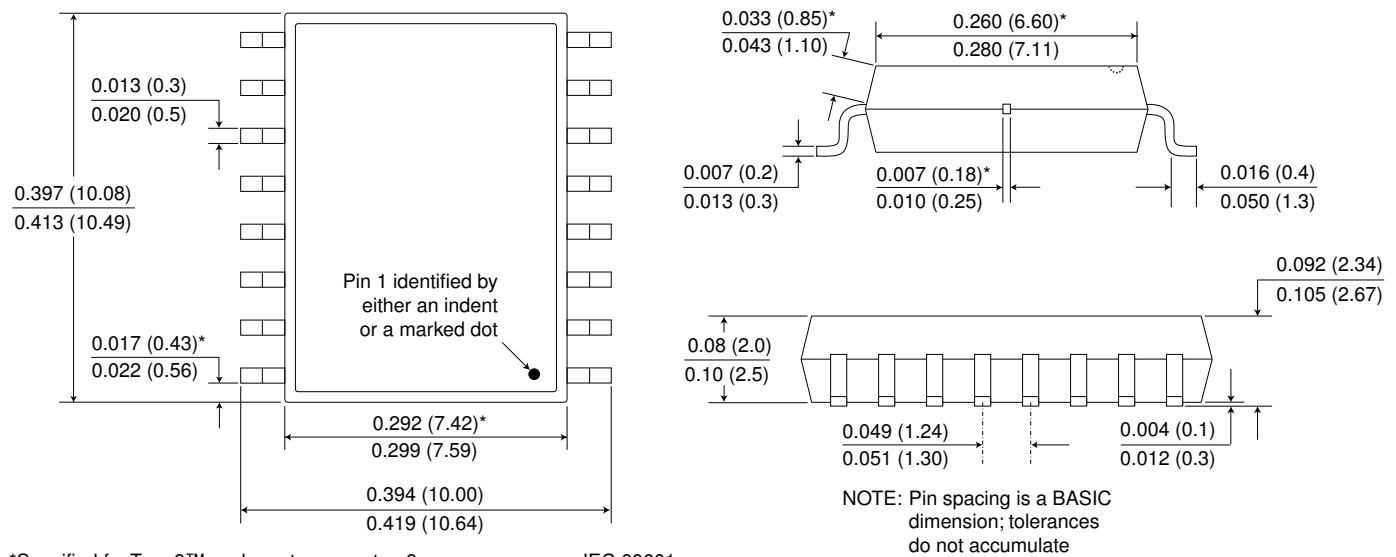
**8-pin SOIC8 Package (IL011-3 / IL012-3)**

Dimensions in inches (mm); scale = approx. 5X



**16-pin 0.3" SOIC16 Package (IL015 / IL016 / IL017)**

Dimensions in inches (mm); scale = approx. 5X



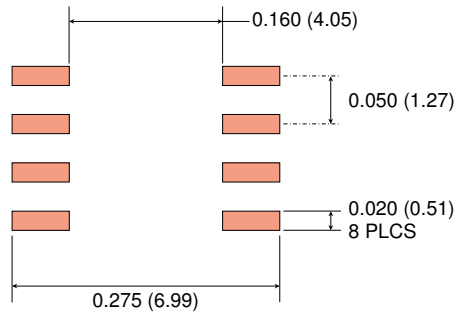
\*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.



**Recommended Pad Layouts**

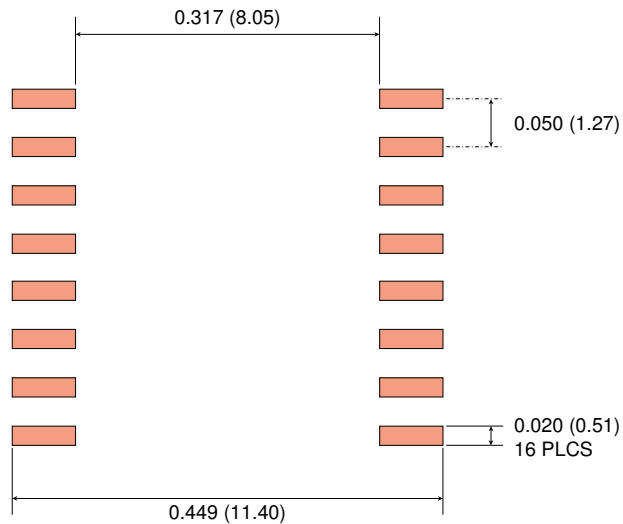
**SOIC8 Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



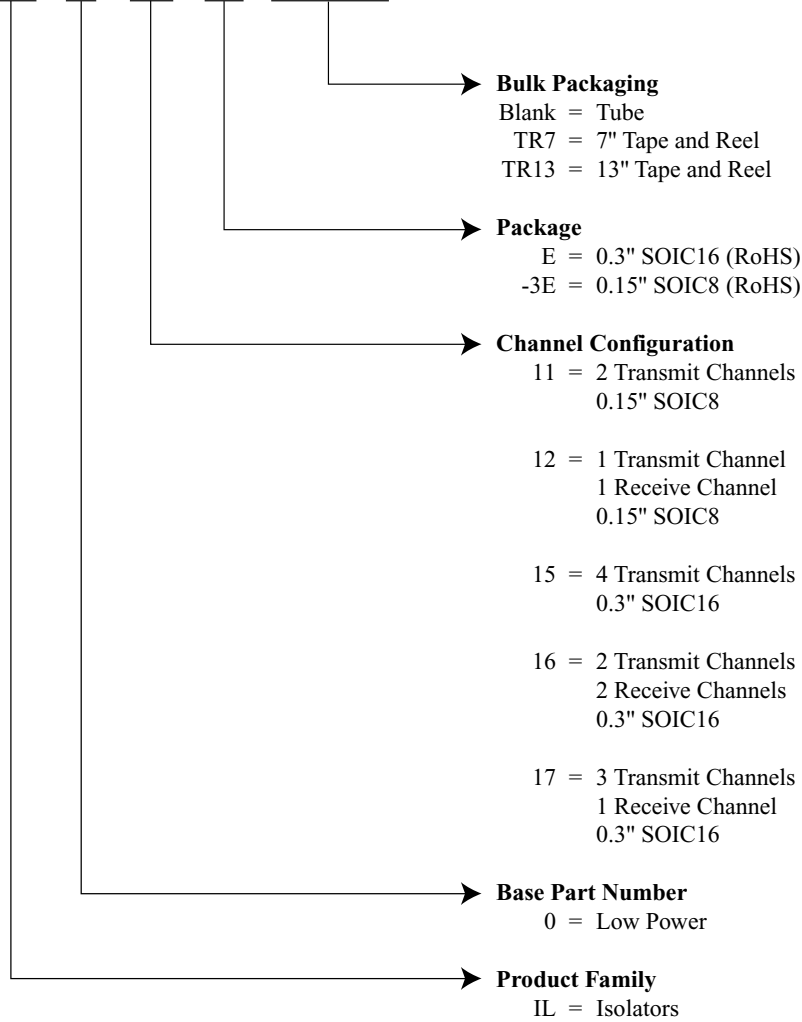
**SOIC16 Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



**Ordering Information**

**IL 0 17 E TR13**



**ISB-DS-001-IL01x-RevB**  
**January 2020**

**Changes**

- Revised thermal characteristics (p. 2).
- Extended power supply range to as low as 2.5 volts.
- Merged 3.3 V and 5 V switching speed specifications and revised specifications (p. 8).
- Upgrade from VDE V 0884-10 to VDE V 0884-11 / IEC 60747-17.
- Updated EMC standards.

**ISB-DS-001-IL01x-RevA**  
**June 2018**

**Changes**

- Added IL011 configuration.
- Decrease typ. Pulse Width Distortion Propagation Delay Skew specs.
- Increase worst-case Propagation Delay specs.
- Product launch.

**ISB-DS-001-IL01x-PRELIM**  
**December 2017**

**Change**

- Preliminary Release.

## Datasheet Limitations

The information and data provided in datasheets shall define the specification of the product as agreed between NVE and its customer, unless NVE and customer have explicitly agreed otherwise in writing. All specifications are based on NVE test protocols. In no event however, shall an agreement be valid in which the NVE product is deemed to offer functions and qualities beyond those described in the datasheet.

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## Applications

Applications described in this datasheet are illustrative only. NVE makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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