

Simple Radiated Emissions Control for NVE's Isolated DC-to-DC Convertors

Powerful Isolated Convertors

Headlined by NVE's ILDC1x-15E, the world's smallest isolated DC-to-DC convertor, NVE offers a family of ultra power-dense isolated power convertors and integrated transceivers and data couplers.

NVE's ILDC1x-, ILDC1xV-, IL4xxx-, and IL7x1xV-series employ isolated DC-to-DC convertors that switch currents up to 400 milliamps at frequencies as high as 110 megahertz. As a result, EMC mitigation techniques are essential to control radiated emissions. Fortunately, NVE's isolated DC-to-DC convertors will pass CISPR Class B (FCC Class B) standards by controlling two sources of radiated emissions: edge emissions and input-to-output dipole emissions. This application bulletin outlines NVE's recommended technique for passing CISPR Class B testing.



At 3 x 5.5 mm, NVE's ILDC1x-15E are the world's smallest isolated DC-to-DC convertors.

Problems with PCB Layout

Figure 1 demonstrates problems caused by a typical four-layer PCB layout. *Edge emissions* are generated when vias carrying high-frequency currents radiate outwards between PCB layers. Without a strong grounding perimeter to enclose and contain the currents, they will penetrate the edge and escape to adjacent PCB layers, creating a large, radiating dipole antenna loop. Poor bypassing capacitor placement creates additional large radiating loops. Additionally, bypass capacitors with poor high-frequency performance will cause higher radiated emissions because they act like antennae for frequency content above their self-resonant frequency.

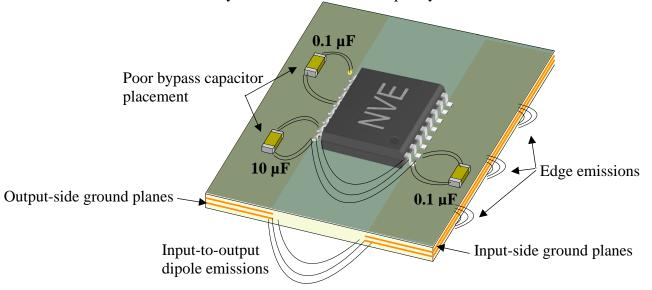


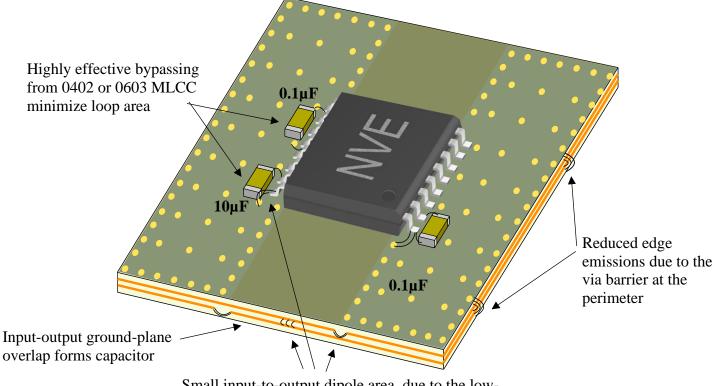
Figure 1: Problems with a standard four-layer PCB layout when designing isolated DC-to-DC convertors. Due to the high-power, high-frequency switching of the convertor, large antenna loops may be created without a mitigation strategy.

Similarly, an *input-to-output dipole* is created by the high-frequency currents crossing the isolation barrier. These relatively large currents have a large loop area shown in Figure 1. To ensure meeting CISPR Class B radiated emissions standards, the loop size can be reduced with proper layout techniques.



NVE Recommended Layout to Pass CISPR Class B the First Time, Every Time

Figure 2 demonstrates NVE's recommended solution for curbing radiated emissions. Stitching vias around the PCB's perimeter form a sturdy ground connection to prevent high-frequency current emissions from breaching the edge of the PCB. To minimize the large input-to-output dipole area, overlapping ground planes on inner layers form a stitching capacitor. Lastly, bypass capacitors are high-quality, low-inductance multilayer ceramics no larger than 0603, and they are placed as close as possible to the pins.



Small input-to-output dipole area, due to the lowimpedance path provided by the stitching capacitor

Figure 2: NVE recommended PCB layout to pass CISPR Class B radiated emissions.

The stackup in Figure 3 demonstrates the recommended stitching capacitance technique. A capacitance of 10 to 20 pF is generally sufficient to control high-frequency radiated emissions.

The capacitance of the overlapping layers can be estimated using the formula for the capacitance of a parallel-plate capacitor: $C = \frac{\epsilon A}{d}$, where $\epsilon = 0.0354$ pF/mm for FR4 PCB material, A is the cross-sectional overlap area, and d is the distance between Inner1 and Inner2 layers.

As an example, Inner1 and Inner2 are commonly spaced 0.5 to 1.3 millimeters apart on a standard 1.6-millimeter PCB. Therefore, the required 10 to 20 pF stitching capacitance can be achieved with an overlap area between 140 and 735 mm². This is the recommended range of overlapping area, with higher capacitance generally curbing emissions to greater degree.



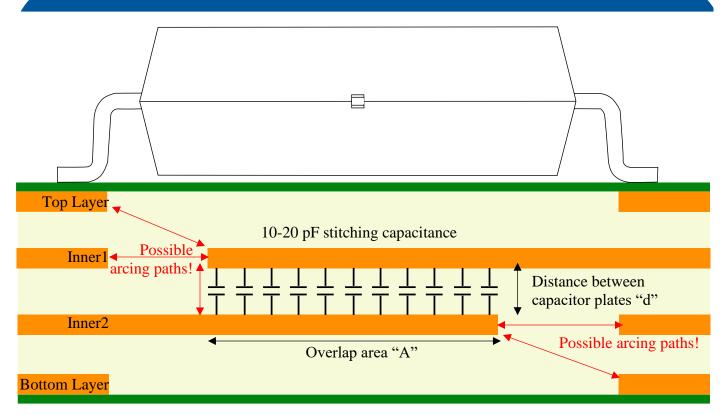


Figure 3: Stackup of four-layer PCB using NVE's recommended stitching capacitance.

Figure 3 also demonstrates a stackup with NVE's True-8 mm creepage, which is required for 250 V_{RMS} working voltage under IEC 60601 (see nve.com/Downloads/ab23 and nve.com/Downloads/ab28).

In addition to maintaining eight-millimeter creepage on top and bottom layers, it is important consider the spacing between ground planes on inner layers. The overlapping planes create a possible arcing path through the FR4 PCB material. FR4 is an insulator, so these possible arcing paths do not detract from the board's creepage specification. But FR4 has a dielectric breakdown voltage of 12 to 36 kV/mm.

The most common source of accidental arcing comes from overlap between Top and Inner1 layers and overlap between Inner2 and Bottom layers. In many stackups, these adjacent layers are as close as 0.1 mm apart. Arcing is possible at only 1.2 kV in these circumstances.

Example landing pattern:

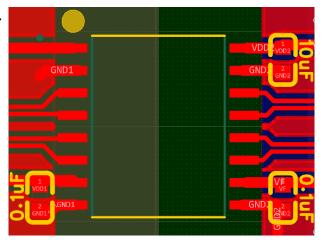


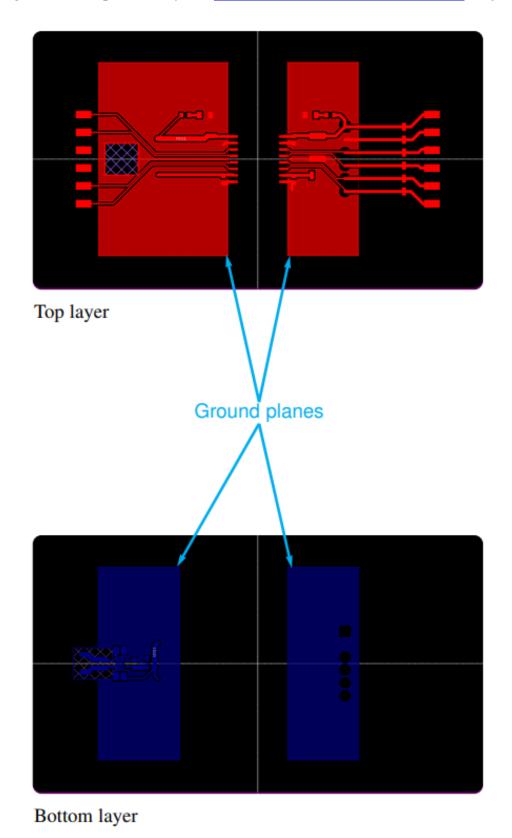
Figure 4: Typical landing pattern for IL7000-Series isolators with integrated DC-to-DC Convertors.

The three required external capacitors are 0402 or 0603 footprint and placed as close as possible to power pins. A stitching capacitor on inner plane layers helps minimize radiated emissions.

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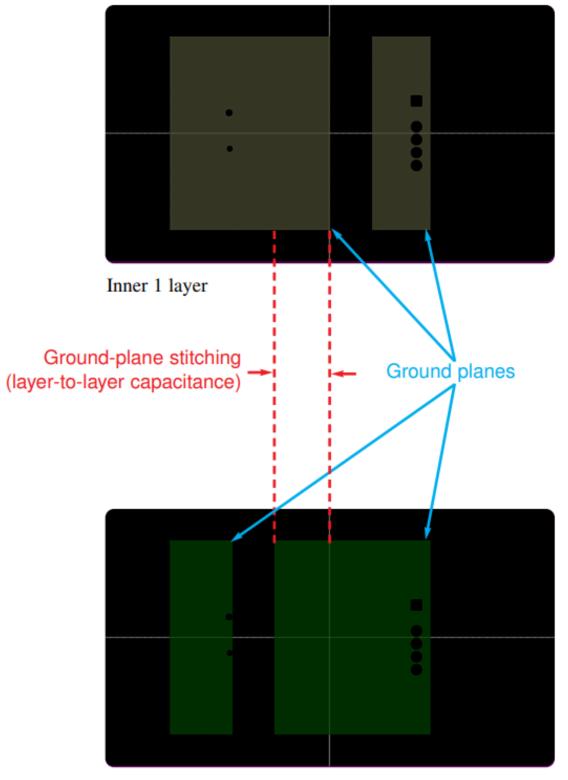
Figure 5: Example PCB layout: NVE's IL7614V-01 Evaluation Board (1 of 2)



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Figure 6: Example PCB layout: NVE's IL7614V-01 Evaluation Board (2 of 2)



Inner 2 layer



Checklist for Worry-free Radiated Emissions Compliance

- ✓ Three external capacitors (required for normal operation), low-inductance MLCC, and 0603 or smaller
- ✓ Four-layer PCB
- ✓ Ground planes on at least three layers in the vicinity of the convertor
- ✓ Perimeter vias to enclose ground planes
- ✓ 10-20 pF stitching capacitor using overlapping PCB layers*
- ✓ Double check the PCB stackup for possible arcing paths from inner layer overlap

Worry-Free CISPR Class B Compliance

NVE DC-to-DC convertors are designed to minimize EMI emissions. The oscillator operates above 88 MHz, where emission limits are higher since there is less risk of interference with common commercial radio and television broadcasting. The high operating frequency reduces the required stitching capacitance and makes overlapping layers practical. Frequency-hopping technology dramatically reduces peak EMI and synchronous rectification and PWM control are avoided, resulting in inherently low EMI. This inherently low EMI eliminates the need for shielding or external mitigation components such as ferrite beads.

Proving EMC compliance is a difficult and costly engineering effort. Don't take chances on isolated DC-to-DC convertors with a reputation for excessive radiated emissions. NVE's isolated DC-to-DC convertors and couplers and transceivers with integrated DC-to-DC convertors will pass every time using the simple mitigation techniques described in this bulletin.

Unmatched EMI Results

NVE's radiated emissions testing results for the <u>IL7614V-01 evaluation board</u> are below for reference:

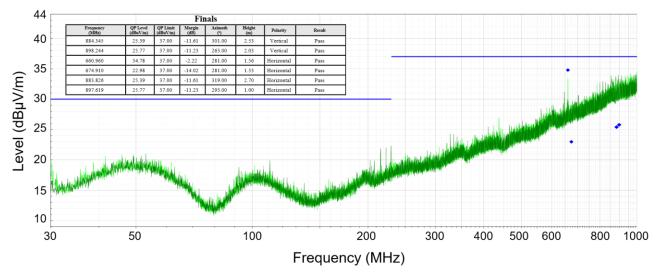


Figure 7: low-frequency radiated emissions data for NVE's IL7614V-01 evaluation board.

^{*}External stitching capacitor components are NOT recommended due to parasitic inductance above one gigahertz. Overlapped PCB layers is the best way to control high-frequency emissions.



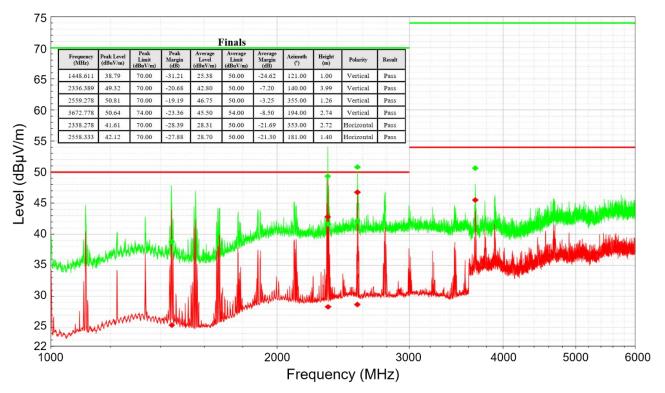


Figure 8: high-frequency radiated emissions data for NVE's <u>IL7614V-01 evaluation board</u>.

Datasheets

- nve.com/Downloads/il71x.pdf
- nve.com/Downloads/il76xx.pdf

Videos and Application Bulletins

- youtube.com/c/NveCorporation
- nve.com/appNotes

Contact Us for Additional Support

- iso-apps@nve.com
- (952) 829-9217

Available parts:

ILDC1x-15E	The world's smallest DC-to-DC convertors
	(3 x 5.5 mm); 1 kV isolation
ILDC1xV-15E	The world's smallest DC-to-DC convertors
	(3 x 5.5 mm); 2.5 kV isolation
ILDC1xVE	High-isolation V-series DC-to-DC convertors
IL7x1xVE	High-isolation V-series digital isolators with
	integrated dc-dc convertors
IL4x85E	RS-485 transceivers with integrated DC-to-
	DC convertors
IL4x22E	RS-422 / RS-485 transceivers with integrated
	DC-to-DC convertors

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