Magnetic tunneling applied to memory (invited)

J. M. Daughton
Nonvolatile Electronics, Inc., 11409 Valley View Road, Eden Prairie, Minnesota 55344

Random access magnetoresistive memories have been designed using anisotropic magnetoresistive (AMR) material and more recently giant magnetoresistive (GMR) material. The thin films in these memories have low sheet resistivities (about 10 Ω/sq), resulting in cell resistances of 10 to 100 Ω at competitive areal densities. High sense currents of a mA or more are required to get signals on the order of a few mV. Spin dependent tunneling (SDT) devices are intrinsically high impedance, with typical equivalent resistance values of 10^4-10^9 Ω for a square micron area. SDT cells have the potential for signals on the order of 10 mV with lower sense currents, and hence, faster access times than GMR memory. A GMR pseudospin valve memory concept is presented for comparison with SDT memory. Three different design approaches are discussed for SDT memory: (1) high-density memory arrays similar to those in AMR and GMR memories, (2) a transistor per cell approach similar to semiconductor dynamic random access memory, and (3) embedded SDT devices in a flip–flop cell similar to semiconductor static random access memory. The conclusions are: (1) SDT memory is potentially higher speed than GMR memory, (2) SDT memory has no area advantage compared with dense GMR memory, and (3) risks with SDT memory include (a) processing ultrathin dielectric layers uniformly and reliably that are compatible with integrated circuits and (b) attaining sufficiently low impedance levels to get a satisfactory signal-to-noise ratio in a small area cell. [S0021-8979(97)56908-8]

I. INTRODUCTION

Working magnetoresistance random access memories (MRAMs) using anisotropic magnetoresistance (AMR) cobalt–permalloy for the magnetoresistive material and complementary metal–oxide–semiconductors for the on-chip circuitry have been demonstrated.[1] These memories are nonvolatile, are read nondestructively, and show no signs of wearout to 10^{15} read or write cycles. The memory arrays in these memories use 2 μm photolithography, and for reasons to be discussed later, sense signals are relatively small (1 mV), leading to a read access time of about 250 ns even though the number of squares (5–6) per cell is relatively large.

Giant magnetoresistance (GMR) materials show promise for higher signal (faster) and higher density (lower cost) MRAMs. Memory cells with GMR spin valves and GMR sandwiches have been demonstrated,[2–5] and there are several active programs on developing GMR memories.

Spin dependent tunneling (SDT) materials offer yet another opportunity for enhanced random access nonvolatile memories. Cells with high impedance and low interlayer coupling could lead to much faster MRAM. This paper will explore how spin dependent tunneling devices might be used for random access nonvolatile memory, and how the resulting memory would compare with GMR memory concepts.

The primary factor determining read access time is the signal-to-noise ratio. A new MRAM cell that can store data at very high densities, and yet give greatly improved signal levels is described in the next section. This concept, the pseudospin valve (PSV) cell, is suitable for either a GMR memory or a tunneling memory. Then the basic properties of tunneling devices are explored, and their relationship with memory cell design is examined. Tunneling designs are then presented and compared with GMR designs. A very important aspect of these memories is compatibility with integrated circuit designs and processes. The outlook for tunneling memory is then summarized.

II. MAGNETORESISTIVE MEMORY CONCEPTS

In magnetoresistive memory, storing data is accomplished by applying magnetic fields and thereby causing a magnetic material in a cell to be magnetized into either of two possible memory states. Recalling data is accomplished by sensing resistance changes in the cell when magnetic fields are applied. The magnetic fields are created by passing currents through strip lines external to the magnetic structure, or through the magnetic structures themselves.

Early MRAM cells were narrow AMR stripes etched into a three layer stack of permalloy–tantalum nitride–permalloy. Data were stored by magnetizing the stripe either clockwise or counterclockwise around a sense current reference. Deposition induced anisotropy was used to make these magnetization states stable. Reading was accomplished by noting the change in voltage across the sense line with the application of magnetic fields along the sense line. These changes in voltage were about 20%–30% of the maximum potential magnetoresistive voltage swing, which made the sense signals relatively small. At smaller dimensions, these signals would become even smaller due to edge curling effects in the cell. At a given noise level, the read access time should decrease as the inverse square of the sense signal. Hence, new modes of operation with higher signals at small dimensions are very desirable for improving read access times for future magnetoresistive memories.

Figure 1 shows a ''pseudospin valve'' or PSV, so named because at low-field values one of the layers could be considered to be pinned while the other is reversible.[6] In this structure, the data are stored in the film with the higher moment (product of magnetization and thickness) film, while the switching of the lower moment layer can be used to

 0021-8979/97/81(8)/3758/6/$10.00

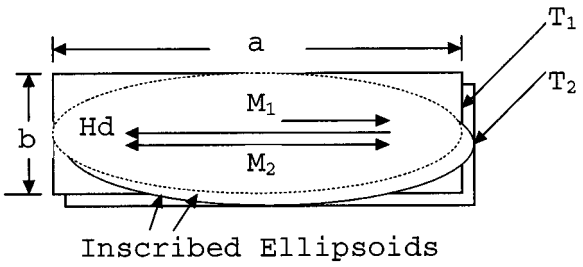

FIG. 1. Pseudospin valve (PSV) memory cell with two thin films of thicknesses T_1 and T_2 and moments M_1 and M_2. The stiffer of the two films stores data, and the softer is reversed during a two cycle read operation. With no external fields, the magnetizations are antiparallel.

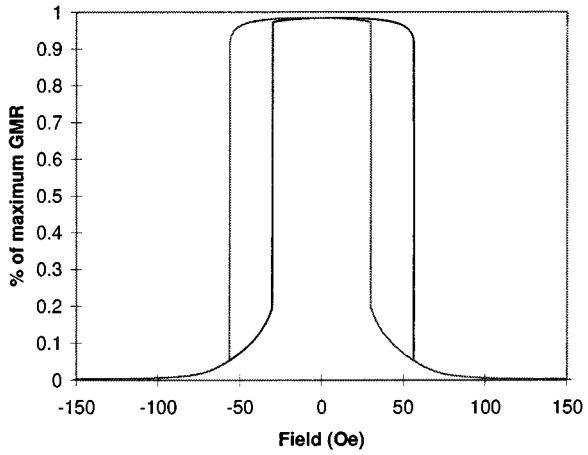

FIG. 2. Magnetoresistance dependence on magnetic field for a 0.2 μm$\times$0.5 μm PSV cell with film thicknesses of 25 and 30 A, 12 000 G magnetizations, a 3 Oe sense field, a 2 Oe parallel material coupling field, and anisotropy fields of 15 Oe for each magnetic film.

modulate the resistance. Shape anisotropy provides the two state energy well for storing ''1''s and ''0''s. The PSV concept could be used with either GMR or SDT structures.

In the rest state the magnetizations in the two layers (M_1 and M_2, with thicknesses T_1 and T_2, respectively) are antiparallel, giving small self-demagnetizing fields and small external stray fields on nearby memory cells, both of which could help with cell stability. When the memory is not being addressed, this cell would have about 1/10 of the stray and self-demagnetizing fields of spin valve cells where the magnetizations can be in the same direction within a cell. With worst case read and write conditions, the demagnetizing and stray field advantages for this structure are still substantial.

A GMR PSV cell with a conductive interlayer provides about 5%–6% GMR, but the bigger advantage of the device is that the signal can be equivalent to a plus 5%–6% for a ''1'' and a minus 5%–6% for a ''0.'' Figure 2 illustrates a projected resistance–filled characteristic for a 0.2 μm$\times$0.5 μm cell with T_1 of 25 Å thick and T_2 of 30 Å thick, both films having magnetizations of 12 000 G. Note that a field of about 40 Oe is not sufficient to switch the hard layer, but switches the soft layer. To read, a positive interrogate 40 Oe field is applied that is sufficient in magnitude to switch the soft layer if it opposes the soft layer's magnetization. Then the interrogate field is reversed, and the change in device resistance noted. The change will then be positive or negative depending on whether a ''1'' or a ''0'' is stored, and the signal swing would be 90% of the maximum GMR in each case. Note that this signal is roughly equivalent to 7.2 times the signal using the same kind of GMR material with the original MRAM designs (12% compared to 6% maximum available times 90% compared to 25% utilization). A similar sensing concept using another GMR structure has been described elsewhere.[7]

The PSV cell requires that the hard layer be switched for writing a bit. In principle, that can be accomplished in a two-dimensional array with coincident currents that supply a magnetic field in the same direction, or with coincident currents that produce fields that are orthogonal. For GMR cells, the sense current could also supply magnetic fields that could aid in switching. Another paper at this conference[6] will discuss the PSV concept in greater detail and provide some experimental data. Differences in thickness of the two magnetic layers having the same composition are shown to determine which is the ''soft'' and which is the ''hard'' magnetic layer. Similar cells using SDT materials are discussed in more detail in Sec. IV.

III. SDT DEVICES

Spin dependent tunneling devices have a number of characteristics that must be taken into account in their use as memory devices. A brief summary of their characteristics as observed by several workers[8–11] follows:

(1) For low values of voltage across the device, the current changes relatively linearly with voltage, but the current changes faster than linearly for higher values of voltage.

(2) The junction magnetoresistance (JMR), or the percentage change in tunneling current due to magnetic fields, ranges from a few percent to about 20%. As the voltage across the device increases, JMR decreases, losing roughly one-half of the low-voltage values at several hundred mV.

(3) The effective magnetoresistance increases to about twice the room-temperature values when the devices are cooled to 77 K but tunneling current increases only about 20%, indicating that the effective resistivity is relatively insensitive (1000 ppm/ °C) to temperature.

(4) The observed resistances of the devices have ranged greatly in value from under 10^4 to over 10^9 Ω μm^2.

(5) The coupling fields between the magnetic layers in the SDT devices are relatively smaller (a few Oe) compared with those between the magnetic layers in GMR magnetic sandwiches with equivalent interlayer thicknesses, where, for example, coupling fields in GMR sandwiches of 20 Oe are common for 20 Å thick copper interlayer.

While most of the reported research concerned relatively large devices deposited through shadow masks, it has been shown possible to deposit both magnetic layers and the barrier layer (aluminum oxide) in one process step, and to use conventional photolithography techniques to form tunneling devices, like those shown in Fig. 3. Thick aluminum copper leadouts are then formed from contacts to the element to

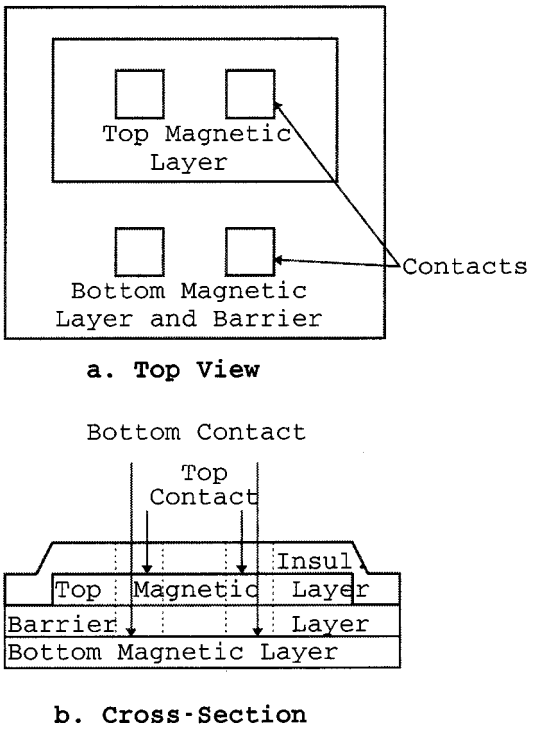

FIG. 3. Schematic diagram of an experimental SDT device processed by photolithography.

large contact pads. Devices as small as 6.5 μm$\times$13 μm were made successfully by this technique. As indicated by Moodera, it is advantageous to leave a thin unoxidized barrier metal between the bottom magnetic layer and the barrier.[8]

Figure 4 shows a resistance–field characteristic for a large 1 mm$\times$1 mm device made in this fashion. This device had modest GMR of 5%, and an equivalent resistance of about 5000 Ω (5×10^9 Ω μm^2). Most of the devices on a 4 in. diam were nearly identical to this one, and it should be noted that each device would have an equivalent area to one million memory cells of one square micron.

An important parameter for tunneling memory is the intrinsic RC time constant of the device. At low voltages, the intrinsic resistance R is on the order of 10^4–10^9 Ω. The capacitance C should be deduced by the thickness and relative dielectric constant (about 8 for aluminum oxide) of the device, and should be approximately

$$\text{Capacitance(F)} = 8.85\times10^{-18}\times8\times10^{-6}\,\text{Area}(\mu\text{m}^2)/s(\mu\text{m}), \tag{1}$$

where s is the thickness of the barrier in microns. The equivalent resistance of the device at low voltages varies much faster than linearly with s as follows:[9]

$$R=(K_1 s)e^{(K_2 s)}, \tag{2}$$

where K_1 and K_2 are material constants. The product of R and C then is exponentially dependent on s, and can be reduced by reducing s until $K_2 s$ is much smaller than 1, or until the processing difficulties with thin barriers prevent further reductions in thickness.

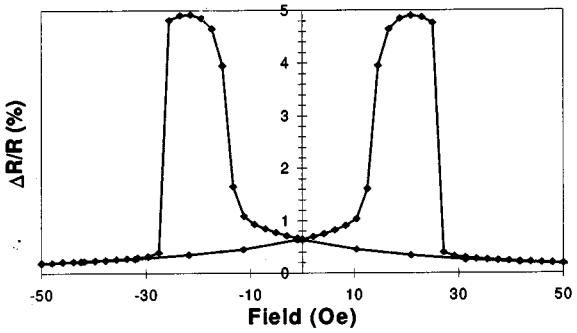

FIG. 4. Typical SDT characteristic for magnetoresistance as a function of field. This sample was 1 mm$\times$1 mm with a cross section of 125 A of 20Co65Ni15Fe–20 A partially oxidized Al and 6A Al_2O_3–125 A of 95Co5Fe and was biased at 100 mV. Its resistance was 5.3 kΩ.

The reason that the RC time constant is important for memory application is because of speed limitations in reading the data from a memory cell. Suppose that data is stored in a SDT cell with a conductance G with magnetizations being antiparallel, and exhibits an increase in conductance of ΔG when the magnetizations are switched to parallel. Suppose the cell is driven by a current source, and a sense amplifier is placed across the cell to detect the change in output voltage when the magnetizations are changed from parallel to antiparallel. Suppose that the input impedance of the amplifier is $1/G$, approximately the maximum energy transfer value for the amplifier.

The voltage across the cell can change instantaneously, but the sense amplifier cannot detect the change instantaneously. The voltage into the sense amplifier will increase from $I_s/(G+\Delta G)$ to an ultimate value of I_s/G, or a change of approximately the initial voltage across the cell times the equivalent MR. The time constant of the signal rise is $C/2G$.

Using a value of 8 for the relative dielectric constant and from 10^4 to 10^9 Ω resistance for the value of a SDT cell 1 μm^2 with a dielectric thickness of 2 nm, the value of C would be about 0.035 pF and the value of RC would be between 0.35 and 35 000 ns. For modern random access memory applications, the equivalent resistance for SDT devices must be at the lower end of the resistance range. It is, thus, very important to make the dielectric thin enough to allow the memory to operate at fast read access times.

IV. SDT CELL DESIGN

SPT cells have already been proposed.[8,9,12] For discussion here, the storage function of a SDT will be proposed using very similar techniques to the GMR PSV memory cells described earlier in this paper. Consider the cell shown in Fig. 5, which functions very much like PSV devices using GMR sandwich materials, except the readout mechanism uses SDT rather than GMR. A good conductor under the SDT device provides one contact to the cell, and the top contact is made through a contact cut in the insulator.

It is interesting to consider some basic signal and noise considerations for a single SDT cell of this type. The signal voltage is limited to approximately the magnetoresistance

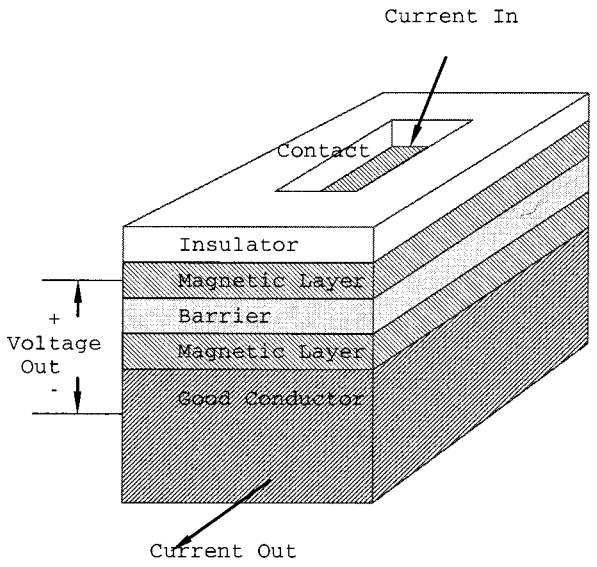

FIG. 5. SDT memory cell with sensing connections. The drive lines for writing are not shown. For high density, two magnetic layers have the same lateral dimensions, possibly presenting a processing difficulty.

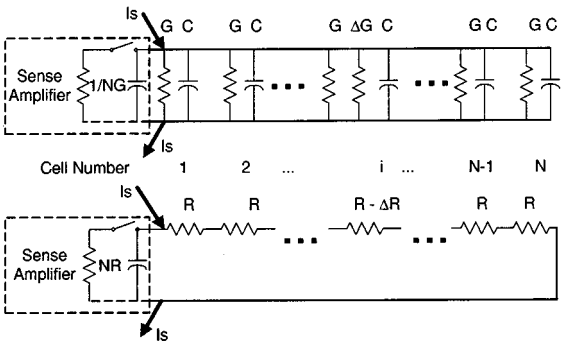

FIG. 6. Parallel connection of SDT cells and series connection of GMR cells.

ratio (MR) times 100 mV (the value of voltage above which the MR drops off). With a 20% MR, the signal would be about 20 mV. The noise is strongly related to the equivalent resistance R of the device and the band width of the sense system used, Δf, and is given at room temperature by

$$Vn = 1.26\times 10^{-10}(F)(R\Delta f\ )^{1/2}. \tag{3}$$

A noise factor F of unity is the lowest theoretical value. In practice, the noise may be considerably higher due to electron interaction with domain walls, for example, and F has been observed to be from near unity up to several orders of magnitude in GMR devices. At this point there is no published noise data on SDT devices, although it is possible that SDT devices are not as sensitive to magnetic noise as GMR devices. If the bandwidth Δf is 100 MHz, then the expression simplifies to

$$Vn = 1.26\times 10^{-6}(F)(R)^{1/2}. \tag{4}$$

Thus, to improve the signal-to-noise ratio, one could make the device larger for lower resistance and lower noise. To obtain a signal-to-noise ratio of 20 (a value sometimes used for memory to obtain a low failure rate), and with a 20 mV signal and a F of 1, the value of Vn would have to be less than 1 mV, and R would have to be less than 890 kΩ. With a 10^9 Ω μm^2 technology, the memory cell would have to be 1122 μm^2 in area, much too large to be competitive with other memory technologies. At 10^5 Ω μm^2, the memory cell would have to be only 0.1 μm^2. Obviously, noise limitations also will be very important in determining the maximum allowable equivalent resistance of SDT structures for memory, even when only one cell is sensed in isolation from other cells in the memory.

The upper portion of Fig. 6 shows the effect of adding N SDT cells in parallel, each with a conductance G and a capacitance C. Also shown is the similar situation for GMR cells added in series on a sense line. These two configurations are entirely analogous, with the additional cells affecting the signal-to-noise ratio and circuit loading in a very similar fashion. In the SDT case, the output voltage signal is reduced by the loading of additional cells, while the noise is reduced by the factor $(1/N)^{1/2}$. In the GMR case, the output signal is $I_s\Delta R$, but the noise increases as $(N)^{1/2}$. The signal-to-noise (S/N) ratios for the two cases are

$$\mathrm{SDT(S/N)} = [(I_s/NG)(\mathrm{MR})/[1.26\times 10^{-6}(F)(1/NG)^{1/2}], \tag{5}$$

$$\mathrm{GMR(S/N)} = [(I_sR)(\mathrm{GMR})]/[1.26\times 10^{-6}(F)(NR)^{1/2}]. \tag{6}$$

The above two expressions then become

$$\mathrm{SDT(S/N)} = [V_0(\mathrm{MR})/[1.26\times 10^{-6}(F)(N/G)^{1/2}], \tag{7}$$

$$\mathrm{GMR(S/N)} = [I_sR(\mathrm{GMR})/[1.26\times 10^{-6}(F)(NR)^{1/2}], \tag{8}$$

where V_0 is the voltage across the sense line.

There are constraints on the drive circuits: in the SDT case, cells may not be added indefinitely because eventually the drive circuit will not be able to supply the required current. Similarly, the GMR sense drive circuit may not be able to supply the voltage required (NRI_s) as N becomes large, or an indefinitely high I_s before electromigration or transistor size becomes limiting. In addition, there is a constraint that V_0 not be above about 100 mV for SDT because JMR decreases above that voltage (at least for published data). Assuming a 100 mV voltage drop per cell for the GMR case, and a JMR value of 20% for SDT and a GMR of 6%, and assuming a $1/G$ value of 10 kΩ, and a R value of 100 Ω, the previous expressions become

$$\mathrm{SDT(S/N)} = 159/(F)(N)^{1/2}, \tag{9}$$

$$\mathrm{GMR(S/N)} = 476/(F)(N)^{1/2}. \tag{10}$$

This set of assumptions would make GMR cell strings about three times better in signal to noise if the noise factors F are equal, and would allow the GMR design to connect nine times the number of cells to a sensing circuit.

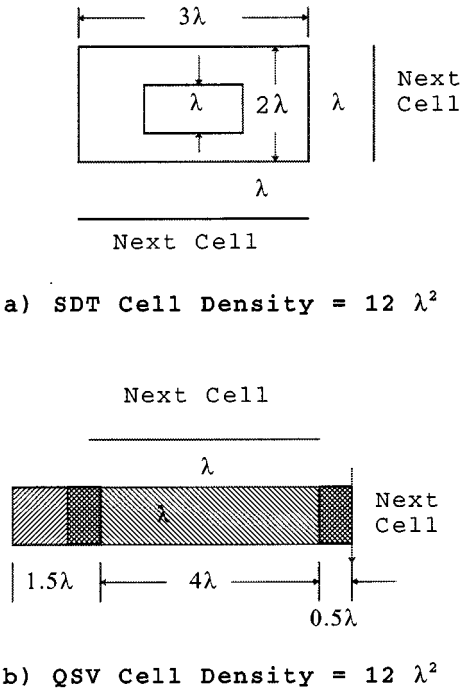

FIG. 7. Representative high-density layouts of SDT and GMR PSV cells, where λ is a length unit for the lithography used.

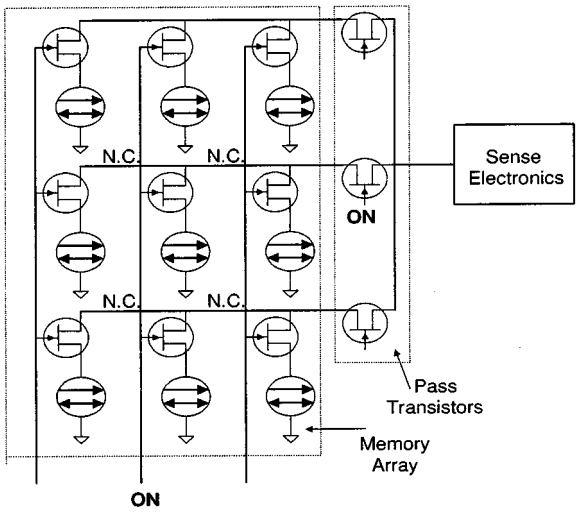

FIG. 8. A 3×3 cell SDT cell array using a transistor per cell. N. C. means a no-connection crossover, and the symbol with inscribed arrows represents a SDT device. Turning on the gates of a column transistor and a row transistor connects the sense electronics to the desired cell. Write circuitry is not shown.

V. SDT MEMORY DESIGN

Three different design concepts are considered. First is a dense array design similar to AMR and GMR memory organizations. Second is a transistor per cell design similar to semiconductor dynamic random access memory (DRAM). Third is a flip–flop concept that uses embedded SDT elements. This cell would operate similarly to semiconductor static random access memory (SRAM).

Figure 7 shows conceptual layouts for SDT and GMR memory cells that use aggressive assumptions for high density. The distance λ is the minimum attainable dimension of linewidths and spacings for the process used. Alignment tolerances of 0.5 λ are assumed. The SDT cell assumes a top contact similar to that shown in Fig. 8. A very large assumption is that the abrupt edges implied by this design can be processed without shorts between the top and bottom magnetic layers. The bottom contact for the SDT cell is assumed to run between cells in a row. The GMR cell has an electrical length of 2.5 λ to 4 λ in order to obtain reasonable signal levels, with shorting bars running between cells.

Only the sense lines are shown. At least two write lines, additional to the sense line, are required for writing a SDT cell. At least one additional write line is also required for the GMR cell. Additional write lines may add area to the cell, but are not considered in Fig. 8. The cell areas as shown are about equal at 12 λ^2 per cell, a cell density which would be competitive with dense DRAM semiconductor memory.

There is no significant density advantage for the SDT design as compared to the GMR design. The use of the sense line for one of the drive lines for switching in the GMR design would be another factor in favor of GMR memory; sense circuitry, and sense selection circuitry occupy a significant fraction of a memory chip, and so having many cells on a sensing node is quite important to density. The signal-to-noise ratio probably favors the GMR design as shown previously, and this enables more cells on a sense line for GMR cells.

Figure 8 shows a block diagram for a transistor per cell SDT memory concept, where the sense electronics is common for an array of cells, and is gated to sense electronics through metal–oxide–semiconductor (MOS) transistors. In Fig. 8, the center cell in the 3×3 array is electrically connected to the sense electronics. As in the previous concept, the write/interrogate lines are not indicated, but are assumed to be separate in a two-dimensional array overlaying the array shown. As noted previously, the signal across the cell would be on the order of 20 mV, and hence, the area and speed of this SDT organization could be on the order of that of DRAM.

Figure 9 shows a flip–flop cell with two SDT devices that would steer the flip flop into the desired state as the circuit is powered up. A pair of PSV elements could be used with one cell written in one state, and the other to the opposite state. The write/interrogate lines are not shown. This type of circuit is very fast (on the order of 1 ns), and it may be possible to make this memory approach the speed of semiconductor SRAM.

SDT devices have an advantage over GMR devices for the last two types of design:

(1) High-density sense electronics has an inherent ''offset'' due to transistor characteristic mismatches and array feature imbalances. These are compensated out of AMR memories and proposed GMR memories with ''auto zero'' circuits, i.e., using circuits that initialize out all imbalances before sensing. The higher values of signal attainable with SDT devices should make it possible to build sense circuits

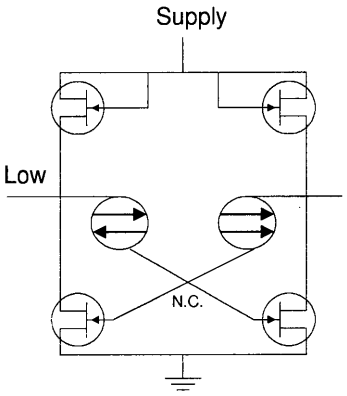

FIG. 9. A flip–flop cell with imbedded SDT devices. One SDT device is writ ten in the high-resistance state and the other in the low state. On power up of the flip flop, it is steered into logic level outputs.

without the auto zero feature, and with reduced gain requirements, thereby improving performance considerably.

(2) Similarly, the sense circuits for the SDT memory do not require high current levels, thus, greatly shortening the settling time required before a signal may be sensed. This would eliminate a substantial portion of the read access time that is unavoidable in AMR and GMR memory.[13]

For the design concepts in Figs. 8 and 9, the size of the SDT devices are not as critical as in Fig. 7 because the transistor area is a much more significant part of the cell area. It would not be as important for the former concepts to make an element that has the abrupt edges and introduces a process risk of shorts between magnetic layers.

VI. INTEGRATED CIRCUIT COMPATIBILITY

There are two aspects to IC compatibility, circuit compatibility and process compatibility. As pointed out in the previous section, the primary difference in electronic characteristics of SDT cells compared with laterally conducting GMR cells is impedance level, with SDT pushing to get down to thousands of ohms and GMR cells pushing to get up to 100 Ω. Integrated circuit impedance levels are intrinsically much closer to those of SDT devices, especially in the case of MOS-based integrated circuits.

Integrating SDT device and integrated circuit processes is necessary for nonvolatile memories. While the integration of AMR and GMR materials with integrated circuits has been demonstrated, it is anticipated that integration of SDT devices with silicon circuits will introduce new challenges, including:

(1) Making reliable contacts to the electrodes without damaging the barrier during the completion of the integrated circuit processing.

(2) Avoiding electrostatic discharges in processing that destroy the barrier. Reactive ion etching and sputtering could both be problem areas.

(3) Developing compatible metallurgies between the SDT and circuits.

(4) Preparing the surface quality of the IC substrates suitable for SDT depositions. The smoothness of dielectrics used for ICs is not an issue for the circuits, but could be a very large one for the SDT device operation.

(5) Temperature durability of the SDT devices must allow for an annealing temperature of about 300 °C to anneal out radiation damage from transistors caused by plasma processes.

VII. CONCLUSIONS

For high-speed nonvolatile memories, SDT devices could potentially out perform GMR devices because their impedance and voltage levels are more compatible with semiconductor devices. A transistor per cell approach or a flip flop with SDT cross-coupling elements should both be feasible. For high-density SDT memories, several additional major hurdles must be overcome to compete with memories using GMR lateral conduction devices, e.g., (1) decreasing the barrier height to achieve an effective resistance of 1–10 kΩ for a 1 μm^2 area for signal/noise ratio, and (2) developing a low-defect process for self-aligned magnetic and barrier layers.

ACKNOWLEDGMENTS

Many useful discussions on SDT devices and MRAM applications with Dr. A. Pohm, Dr. R. Beech, Dr. D. Wang, Dr. B. Everitt, and John Anderson, all of Nonvolatile Electronics, Inc., and with Dr. G. Prinz of NRL and Dr. J. Moodera of MIT, and with A. Hurst of Honeywell are gratefully acknowledged. Much of the research described in this paper was sponsored by NRL, NSF, and DARPA.

[1] G. B. Granley and A. T. Hurst, Proceedings of the Sixth IEEE International NonVolatile Memory Technology Conference in Albuquerque, 138, June, 1996, Publication 96TH8200.
[2] J. M. Daughton, Paper presented at 88th Topical Symposium and 8th Meeting of Specialist Group of Magnetic Multilayers of the Magnetics Society of Japan, Hamnako Lake, January, 1995.
[3] D. D. Tang, P. D. Wang, V. S. Speriosu, S. Le, and K. K. Kung, IEEE Trans. Magn. **31**, 3206 (1995).
[4] Z. Wang and Y. Nakamura, J. Appl. Phys. **79**, 6639 (1996).
[5] J. M. Daughton, Thin Solid Films **216**, 162 (1992).
[6] B. A. Everitt, A. V. Pohm, and J. M. Daughton, Paper No. BD-11 to be presented at MMM Conference in Atlanta, Nov. 12, 1996.
[7] A. V. Pohm, B. A. Everitt, R. S. Beech, and J. Daughton, Proceedings of the Sixth IEEE International NonVolatile Memory Technology Conference in Albuquerque, 113–115, June, 1996, IEEE Publication 96TH8200.
[8] J. S. Moodera, L. R. Kinder, T. Wong, and R. Meservey Phys. Rev. Lett. **74**, 3273 (1995).
[9] T. Miyazaki and N. Tezuka J. Magn. Magn. Mater. **151**, 403 (1995).
[10] R. S. Beech, J. Anderson, J. Daughton, B. A. Everitt, and D. Wang, IEEE Trans. Magn. **32**, 4713 (1996).
[11] J. G. Simmons, J. Appl. Phys. **34**, 1793 (1963).
[12] Z. Wang, and Y. Nakamura, IEEE Trans. Magn. **32**, 4022 (1996).
[13] K. Ranmuthu, A. Pohm, J. Daughton, and C. Comstock, IEEE Trans. Magn. **29**, 2593 (1993).