Effect of Resistance-Area-Product and Thermal Environment on Writing of Magneto-Thermal MRAM

J. G. Deak, *Member, IEEE*, J. M. Daughton, *Member, IEEE*, and A. V. Pohm, *Member, IEEE*

***Abstract*— Blocking temperature written magnetic random access memory element test structures of various sizes and tunnel barrier resistance area products were fabricated in order to study the dependence of writing efficiency and tunnel junction integrity on the thermal environment of the memory element and tunnel junction resistance area product. The test structures were programmed using a CPP writing mode, where the device is heated by passing a small current through the tunnel junction. The device is then field cooled to set the direction of an IrMn/NiFeCo storage layer. Quasi-static write current was measured as a function of resistance area product and for underlayers with differing thermal conductivities. Linear fits to the size dependent write current data suggest that properly designed submicron bits can be written quasi-statically at < 100 μA. Write current for a fixed thermal environment was found to depend inversely on resistance product, but too large a resistance area product causes the tunnel barriers to fail before the memory element can be heated above the blocking temperature of the storage layer. In addition, if the thermal conductivity between the magnetic tunnel junction and substrate is too small, the magnetic tunnel junction will fail before the blocking temperature is reached, even at very low resistance area product values. Proper device design should thus optimize cell thermal resistance and tunnel junction resistance for both reliability and minimum power consumption.**

***Index Terms*—thermally-assisted writing, magnetic random access memory, blocking temperature, magnetic tunnel junction**

I. Introduction

One difficulty in developing high-density magnetoresistive random access memory (MRAM) lies in developing a memory element with long data retention time and low error rates that can be programmed with low currents so that the semiconductor die size will be small enough to make the memory competitive on a cost basis with other non-volatile memory technologies. These problems result in part from an increasing sensitivity to thermal activation as MRAM is scaled to smaller dimensions reducing the energy required for reversing the magnetization of the memory element. In order to improve stability as MRAM element dimensions are reduced, increases in magnetic anisotropy or magnetic volume are required. Unfortunately, most methods used to increase thermal stability at small device dimensions increase programming fields and currents to impractical levels.

There is currently considerable interest in magneto-thermal (MT) writing of MRAM in order to increase memory density, while maintaining long data retention and managing power consumption. In this scheme, Joule heating is used to heat a high stability memory element above an ordering or blocking temperature. At the elevated temperature the energy barrier for reversing the magnetization of the data storage layer is reduced, significantly lowering the field and thus current, required to set the magnetization of a data storage layer. Two schemes are common: One called Curie temperature (T_C) writing, uses a low T_c ferromagnet with shape anisotropy for a storage layer. [1] On heating, the magnetization of the storage layer becomes small as T_c is approached, reducing the coercivity of the storage layer. Another common approach is called blocking temperature (T_B) writing, where the storage layer is a coupled ferromagnet/low T_B antiferromagnet bilayer. [1],[2] In T_B writing, data is stored in the direction of the pinning field of the storage layer resulting in extremely high stability and field immunity. Because shape anisotropy is not required, T_B written MRAM is also potentially higher density then T_c written MRAM. This work focuses on T_B-written MRAM, but many of the conclusions also apply to T_c written MRAM.

Early MT-MRAM work demonstrated the feasibility of thermally assisted writing and focused on Joule heating using a conductor in the plane of the substrate. [1] This is often referred to as a CIP mode. There are drawbacks to the CIP method. If the heating element is shared as required for a high-density device, switching field distributions at the elevated write temperature need to be tightly controlled. This is difficult, and potentially no better than conventional cross-point MRAM. Alternatively, if the memory elements are heated individually to avoid the half-select issue, then vias for the heating conductor make the cell size large resulting in a low density device. An optimal geometry would heat an individual memory element by passing current vertically through the memory element. To this end, a current perpendicular to the plane (CPP) of the substrate Joule heating mode utilizing the tunnel barrier of a magnetic tunnel junction

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(MTJ) as a resistive heater has been demonstrated. [2,3] The CPP mode permits the fabrication of very high density MRAM if the heating current can be reduced below 100 μA to permit a minimum sized select transistor. [4] The difficulty with the CPP mode is MTJ reliability. MTJs generally breakdown when the voltage stress across the tunnel barrier exceeds a few volts, greatly restricting the amount of heating power that can safely be produced. This work thus focuses on an experimental study of the effect of the thermal environment and the resistance area product (RA) of an MTJ on reliability and minimum required heating current of CPP T_B-written MT-MRAM.

II. Experimental Details

A. Sample preparation

Various T_B-written MT-MRAM cells with dimensions ranging from sub-micron to several microns were fabricated on 2000 Å silicon-nitride coated silicon wafers. The magnetic stack used for these devices is optional Cu(200)/Ru(4)/IrMn(4)/NiFeCo(5)/ox-Al(x)/NiFeCo(5)/Ru(4) /Ta, where thickness is given in nm. The cells were patterned by ion milling through to the IrMn layer. In the case where the Cu is omitted, the Ru layer serves as the lower read conductor. Pre-oxidized Al thickness ranged from 6 to 9 Å, with resulting RA ranging from 500 Ωμm^2 to over 1M Ωμm^2. The thermal resistance between the MTJ and substrate is much lower for the devices build on Cu.

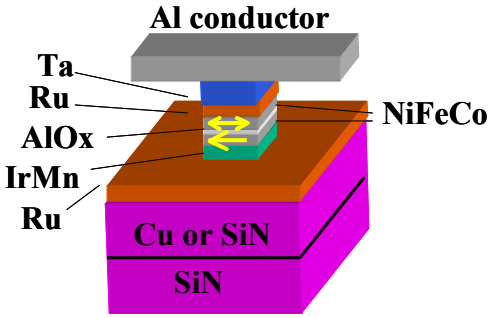

Fig. 1. Thermal MRAM cell. Current passed through the AlOx heats the IrMn/NiFeCo storage layer. The top conductor is 750 nm thick by 4 μm wide Al, and bottom conductor is a Ru plate.

B. Measurement Technique

Figure 1 shows the structure of MT-MRAM cells used for this study. The storage layer is a bottom pinned IrMn/NiFeCo bilayer. A NiFeCo freelayer is used to query the state of the storage layer. Heating and read current are applied between the Al conductor and bottom Ru plate. Four-point measurement is used for reading the resistance of the memory cell.

Quasi-static writing is accomplished by applying a 1 s long current pulse through the tunnel barrier of the MTJ in the presence of an applied field of 250 Oe. This causes the MRAM cell to heat and field cool. The direction of the applied field during cooling determines the set direction of the storage layer. T_B for the 35 Å IrMn layer is 110 C and room temperature is 20 C. The heating current required for reversal thus corresponds to a 90 C temperature rise.

III. Results

Figure 2 shows read signals of a properly functioning device after writing the storage layer in two different orientations. When cooled in a positive field, low resistance occurs at positive fields. When cooled in a negative field, low resistance occurs at negative fields. In a properly optimized T_B-written MT- MRAM element, the high and low resistance values are not affected by the write operation.

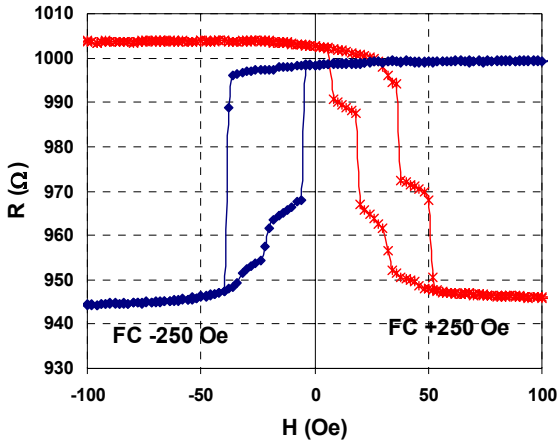

Fig. 2. Magnetoresistance of a properly designed 1 μm cell after programming with ± 250 Oe field using a heating current of 1.75 mA.

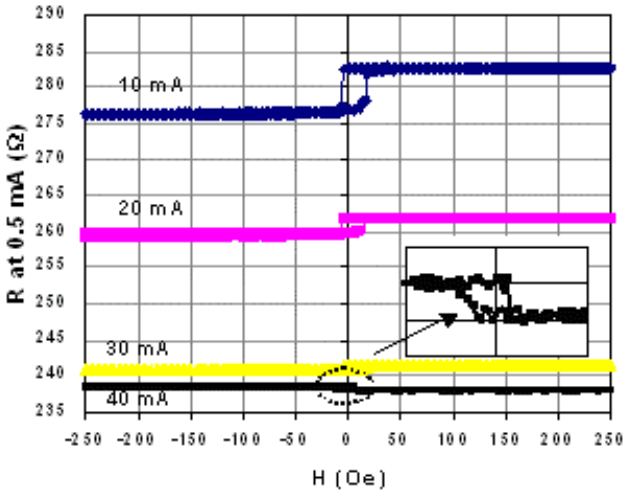

Fig. 3. Deterioration of an MTJ during writing in an improperly designed magneto-thermal MRAM element. The resistance of the MTJ is measured at 0.5 mA, after each attempted heating cycle. The inset shows the magnetization was finally reversed at 40 mA of heating current, at much higher current than the barrier could handle.

Figure 3 illustrates breakdown of the tunnel barrier in a large improperly optimized T_B MT-MRAM cell. The different traces in the plot are measured at low current after heating and field cooling using a sequence of increasing heating currents. The resistance of the device decreases after each attempted write. The magnetization of the storage layer

was not reversed until the tunnel barrier resistance was significantly reduced. This is a typical failure scenario for MT-MRAM. In the work that follows, it is shown that the difference in the behaviors shown in Figs 2 and 3 relates to the thermal insulation between the MTJ and substrate and the resistance area product (<RA>) of the MTJ.

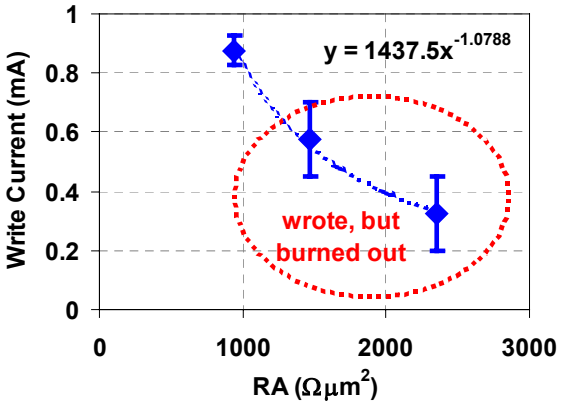

Figure 4. Write current for three different 1 μm x 1 μm magneto-thermal MRAM elements as a function of <RA>. Writing current decreases as 1/<RA>, but large <RA> causes the MTJ to breakdown before the blocking temperature of the storage layer can be reached.

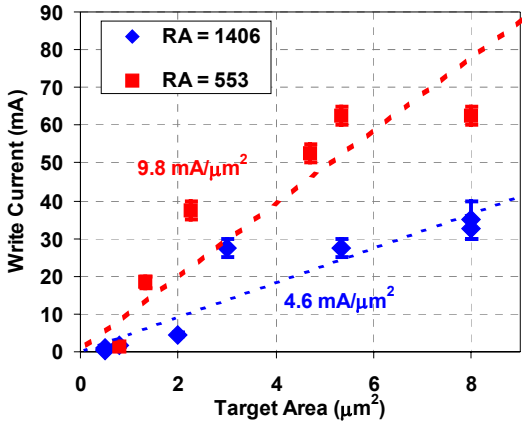

Figure 5. Memory element size dependence of the quasi-static heating current for MTJs with different RA values. Note that increasing RA increases writing efficiency. Extrapolation to 100 nm dimensions shows that high density T_B MRAM devices can be heated very efficiently using less than 100 μA of quasi-static heating current.

Figures 4 and 5 illustrate the effect of <RA> on writing efficiency and MTJ reliability. Heating current is expected to vary as $i_{wrt} = A\sqrt{\Delta T 2K / L\langle RA\rangle}$, and the safe voltage limit should be $\sqrt{\Delta T 2K\langle RA\rangle / L} < V_b$, where L is an effective length of the thermal path between the barrier and heat sink, ΔT is 90 C, K the thermal conductivity, and V_b the breakdown voltage of the barrier. The fit in Fig. 4 and the different slopes in Fig. 5 demonstrate that the heating current decreases as $i_{wrt} \propto \langle RA\rangle^{-1}$, rather than as $\langle RA\rangle^{-1/2}$. Perhaps this means the barrier is the dominant thermal resistance between the IrMn and top Al conductor in this test structure and increasing <RA> results from increased oxidation that reduces the K of the AlOx. In any case, increasing <RA> value lowers the required heating current. Unfortunately, increasing <RA> too much results in a device that cannot be written without destroying the MTJ, consistent with the V_b limit equation.

wafer	Cu?	t Al	Avg RA	Max MR	avg V_b	V_b^2/RA	I_{wrt}/A
		Å	Ωμm²	%	V	mW/μm²	mA/μm²
230	No	6	695	10.8	1.22	2.1	9.8
305	Yes	6	25.0	4.79	0.47	8.8	Can't write
366	Yes	7	200	13.7	0.26	0.34	Can't write
542	No	7	1411	9.19	6.05	26	4.6

TABLE 1. Summary of thermal writing results as a function of RA. The Cu column indicates the presence of the Cu underlayer.

Table 1 shows the effect of the thermal conductivity of the underlayer on device reliability. The table summarizes magnetoresistance (MR), V_b, maximum safe power density in the barrier (V_b^2/RA), and programming current. The devices using only a 40 Å thick Ru bottom electrode did not degrade in this experiment. The devices using a Cu/Ru bottom electrode burn out well before reaching T_B of the storage layer. Vb^2/RA shows this is due to the thermal conductivity of the Cu underlayer: Cu underlayer wafer 305 could not be written, yet it has 4x higher V_b^2/RA than SiN wafer 230, which could be written.

IV. Conclusion

CPP writing of T_B-MRAM was performed as a function of <RA> and thermal conductivity of the cell. Size dependence of the write current suggests submicron bits can be written at < 100 μA. Write current for a fixed thermal environment is found to decrease as <RA> is increased, but too large an <RA> value causes devices to burn out. If the thermal conductivity between the MTJ and substrate is too small, the MRAM cells will burn out before T_B is reached. Proper device design should optimize cell thermal resistance and <RA> for both reliability and efficiency.

Acknowledgment

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