Thermal Management: Best Practices for NVE's Integrated DC-DC Converters

NVE's IsoLoop® technology is enabling the next generation of miniaturization with the world's smallest isolated DC-DC converters and families of isolated data couplers and transceivers with integrated DC-DC converters.

The ILDC11 is a fully-regulated, quarter-watt, 3.3V-to-3.3V DC-DC convertor with 2.5 kV_{RMS} isolation. At 3.0 x 5.5 x 0.9 mm, it is the smallest power converter in its class, and it operates over the full –40°C to 125°C temperature range. Combining high-performance power conversion and ultraminiature size requires care to manage heating, both for the system's performance and the device's operation.

NVE's DC-DC converters use a high-temperature process allowing up to 175°C operating junction temperature, and leveraging NVE's unique packages with simple PCB layout guidelines maximize the device performance and minimize system-level thermal footprint. This bulletin outlines important strategies for board-level thermal management and cost/performance optimization.

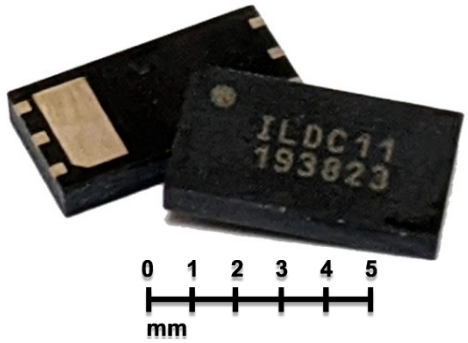

Figure 1. The ILDC11 is an ultraminiature DC-DC converter with custom DFN package and exposed heatsink for efficient heat transfer.

PCB Design for Minimum Junction Temperature

Managing heat dissipation in power conversion systems is a critical aspect of successful system design. High power density devices such as the ILDC11 will markedly benefit from efficient thermal layouts, enabling maximum system reliability with minimal or no thermal derating. In general, the package construction, package interface to board, and board geometry all regulate heat transfer from the hot internal package junctions to the ambient environment.

The thermal resistance, θ, describes the ability to transfer heat across an interface in the presence of a temperature gradient:

$$\theta = \Delta T / P \quad \text{(Eq. 1)}$$

where ΔT is the temperature difference between two points, and P is the power dissipated by the device. A good thermal design minimizes the total thermal resistance between the package junctions and the ambient environment to efficiently remove heat. The junction-to-ambient thermal resistance, θ_{JA}, determines the maximum operating temperature of a device, based on its rated maximum junction temperature and power consumption.

Device	PCB Layout	Max. Junction Temperature*	θ_{JA}	Typ. Max Power	Max. Operating Temperature
ILDC11	Two-sided	175°C	52.5 °C/W	1 W	175°C
ILDC11	2s2p	175°C	46 °C/W	1 W	125°C
IL4685/IL4622	Two-sided	160°C	67 °C/W	1.5 W	60°C
IL4685/IL4622	2s2p	160°C	46 °C/W	1.5 W	90°C**

*IL4685/IL4622 contain GMR elements with maximum junction temperatures of 140°C but are separated from the DC-DC converter junctions by a 14 °C/W thermal resistance.

**IL4685/IL4622 maximum recommended operate temperature is 85°C.

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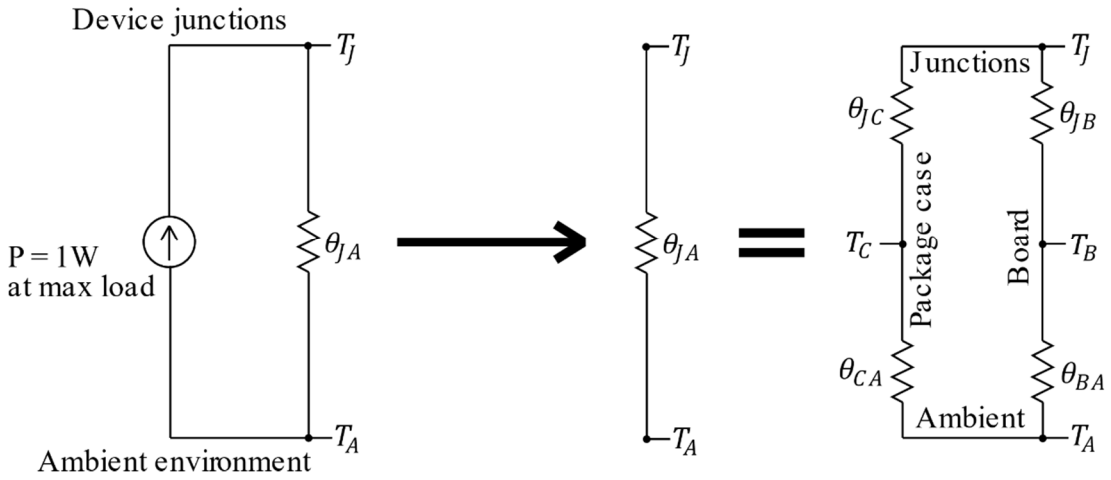

Figure 2. A simplified thermal circuit to model heat transfer in NVE's DC-DC Converters. The circuit nodes are labelled with their respective temperatures between the thermal resistances.

θ_{JA} is determined by the device packaging, PCB layout, and ambient conditions. The thermal circuit in Figure 2 illustrates the composition of θ_{JA} in a typical ILDC11 application. The junction-to-board and board-to-ambient interfaces are controlled by PCB layout, and the junction-to-case and case-to-ambient interfaces are controlled by device packing and ambient airflow.

Basic physics illustrates the design principles to minimize θ_{JA}. The junction-to-board thermal resistance, θ_{JB}, is determined by thermal conduction:

$$P = \kappa \cdot a \cdot \Delta T / \Delta x \quad \text{(Eq. 2, Fourier's Law)}$$

where κ is the interface's thermal conductivity, Δx is the path length, and a is the interfacial area. The thermal resistance can be written as

$$\theta_{JB} = \frac{\Delta x}{\kappa \cdot a} \quad \text{(Eq. 3)}$$

which furnishes the following guidelines for efficient thermal transfer in PCB design:

- Maximize the surface area of the package heatsink connection.
- Minimize the distance from the hot package connection to the heatsink.
- Use material with high thermal conductivity. There are typically four options, and copper is the best where possible.

Material	κ (W/ m · K)
Air	0.024
FR-4	0.34 to 1.1
Nonconductive via-fill epoxy	0.5 to 35
Copper	385

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Board-to-ambient, θ_{BA}, and case-to-ambient, θ_{CA}, thermal resistances are determined by both convective and radiative heat transfer

$$P = h \cdot A \cdot \Delta T \quad \text{(Eq. 4, Newton's Law of Cooling)}$$

$$P = \epsilon \cdot \sigma \cdot A \cdot T^4 \quad \text{(Eq. 5, Stefan-Boltzmann Law)}$$

where h is the convective heat transfer coefficient, ϵ is the emissivity, σ is a constant, and A is the surface area. These transfer mechanisms rely on ambient conditions such as airflow and PCB area and are not always easy to control.

In practice, forced air cooling is the best method to keep system and device temperatures down. When this is not possible or limited, care should be taken to follow the PCB layout guidelines given above. A 2s2p PCB with high-density thermal vias connected to ground is sufficient to operate the ILDC11 and other DC-DC converter products over their full ambient temperature range. Using a single ground plane slightly increases the junction temperature relative to the 2s2p case, but it is a viable solution if minor performance derating is tolerable. Electrically isolated power planes will improve thermal performance in these cases.

Heat Transfer Modeling of the ILDC11 and IL4685

Finite-element temperature models demonstrate the most important layout features for thermal performance. Figure 3 illustrates the successive junction temperature reduction for the ILDC11. A single thermal ground tied to the DAP with thermal vias provides the largest impact, followed by a second thermal ground and small ground plane area increases. Remaining factors result in a less than three percent decrease in T_J, suggesting the system approaches dissipation equilibrium primarily with thermal ground usage. Figure 3 (left) shows the heat flux (arrows) and temperature (color scale) of the ILDC11 QFN package with the DAP connected to two 50 x 40 mm ground planes on a 2s2p circuit board. The total power dissipation in the simulation is maximized for effect at P ≈ 0.90 W, the ambient temperature is 20ºC, and still-air is assumed ($h = 10\ W/m^2K$). With these features, the simulated junction temperature reaches 60ºC.

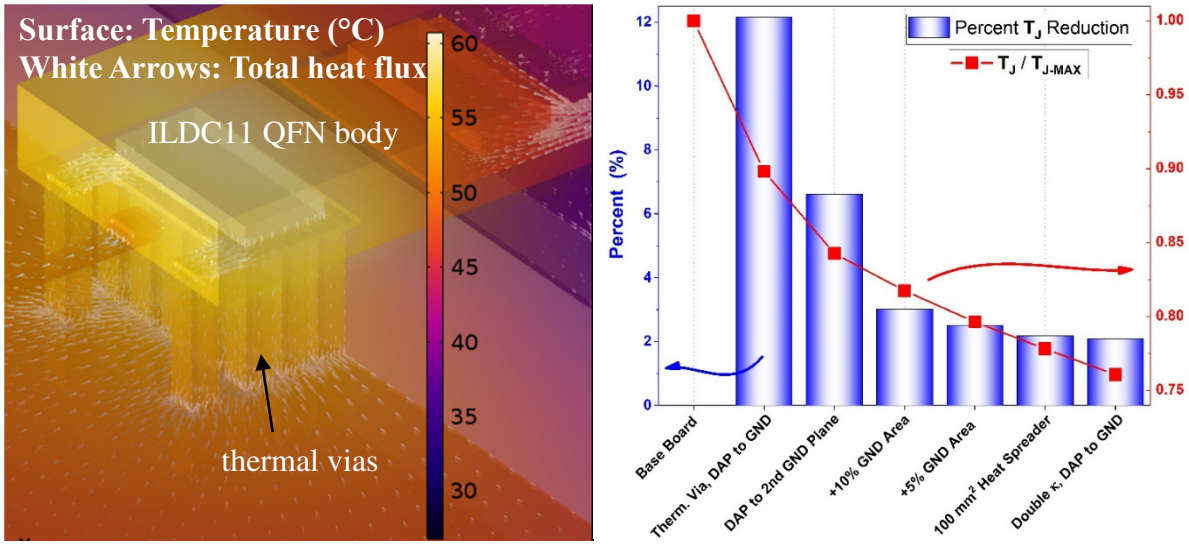

Figure 3. Finite-element model results of heat transfer in the QFN package of the ILDC11 on a 2s2p board (left) and exploration of thermal impacts for various board features (right). Simulations highlight the importance of thermal via to ground plane connections to minimize T_J for optimal heat dissipation.

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Similar results follow for the IL4685E, IL4622E and other isolators with integrated DC-DC converters. IL4600-series parts are packaged in a 16-pin wide body SOIC with two ground pins on the controller side. While there is no exposed DAP, these pins still allow significant conductive heat transfer to thermal ground if used in conjunction with a thermal via scheme and a 2s2p board, similar to the ILDC11. This mimics the θ_{JB}, θ_{BA} minimization in Figure 3. Figure 4 shows a simulated 1.5 W dissipation on a two-sided PCB, with thermal vias on the controller side ground pins. The maximum junction temperature increase is 67ºC (Figure 4, left). As expected, the thermal vias direct significant heat flow away from the internal DAP into the thermal ground sink (Figure 4, right).

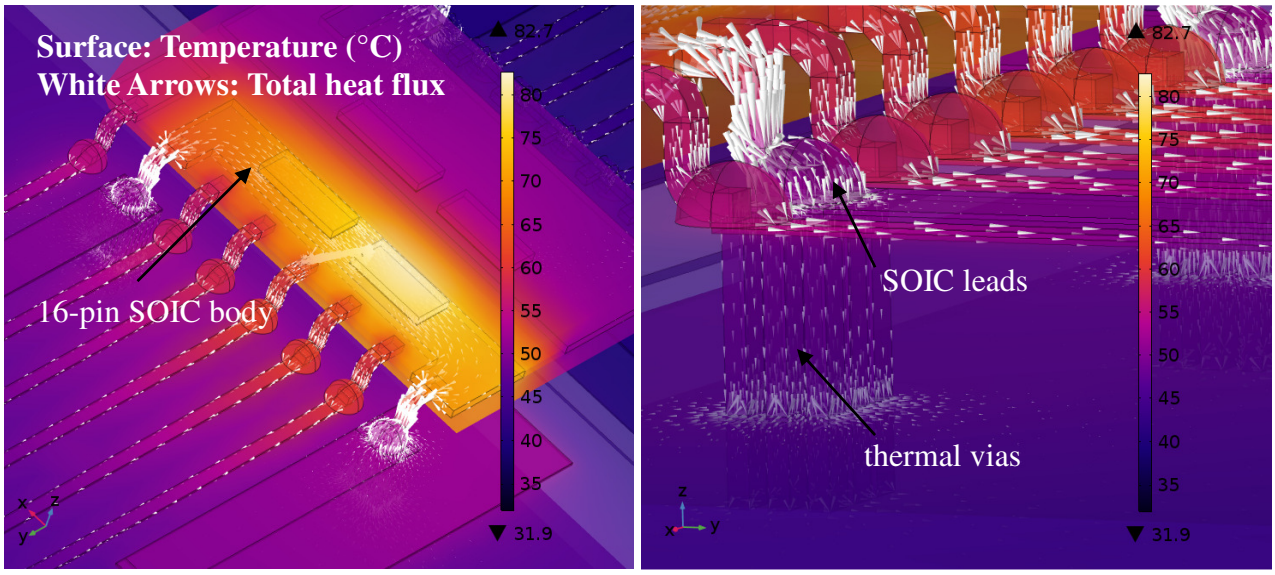

Figure 4. Heat transfer model results for 16-pin wide body SOIC transceivers with integrated DC-DC converter IC's.

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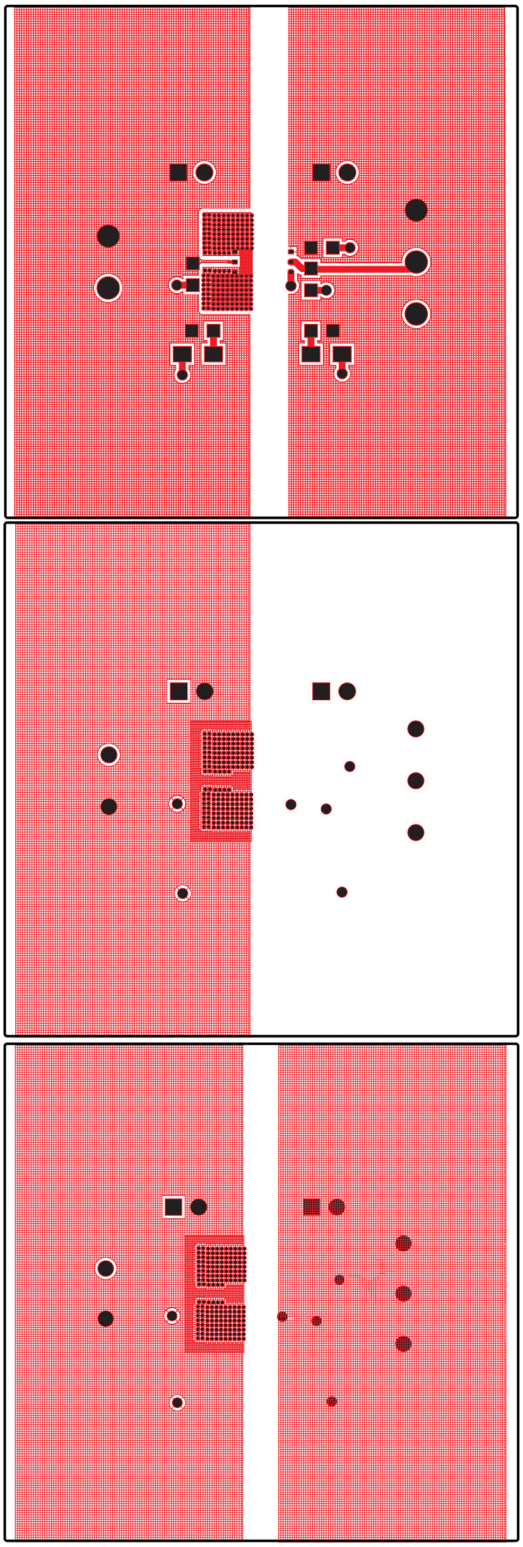

Figure 5. ILDC11-01 Evaluation PCB Layout. Top: top layer. Middle: inner layers. Bottom: bottom layer.

Example: ILDC11-01 Evaluation Boards

NVE offers evaluation boards that demonstrate cost-effective implementations of good thermal design. The ILDC11-01 is a four-layer 2s2p-style board with a dense array of thermal vias in close proximity to the DAP connection on the input side.

The top layer is a mixed signal/power plane layer separated by the isolation barrier. Two inner layers have ground planes on the input side. The bottom layer is the ground plane layer on both sides of the isolation barrier.

The board has two-ounce copper outer layers and one-ounce copper inner layers. One-ounce copper outer layers can be used in some cases to save cost. Double sided boards in this configuration can be used, and two-ounce copper is recommended in these instances.

Designers do not need to allocate the entirety of the inner layers to an electrical ground-plane connection. For standard four-layer boards, it is recommended to allocate a fraction of each layer to thermal management. This fraction can be limited to areas near the thermal via array on the device input side. A good rule-of thumb is to allocate one square-inch of copper for thermal spreading on each layer.

There are 188 ten-mil thermal vias at an 18 mil center-to-center spacing. This is a standard technology for board houses, and it avoids higher-cost via-in-pad processes. The most important factor in designing the thermal vias is to make a large surface area for thermal conduction (see Eq. 2 above). With one-mil through-hole plating, this design has about

$$188 \cdot \pi \cdot \frac{(10^2 - 9^2)}{4} = 2805 \text{ mil}^2$$

of copper surface area to conduct the heat.

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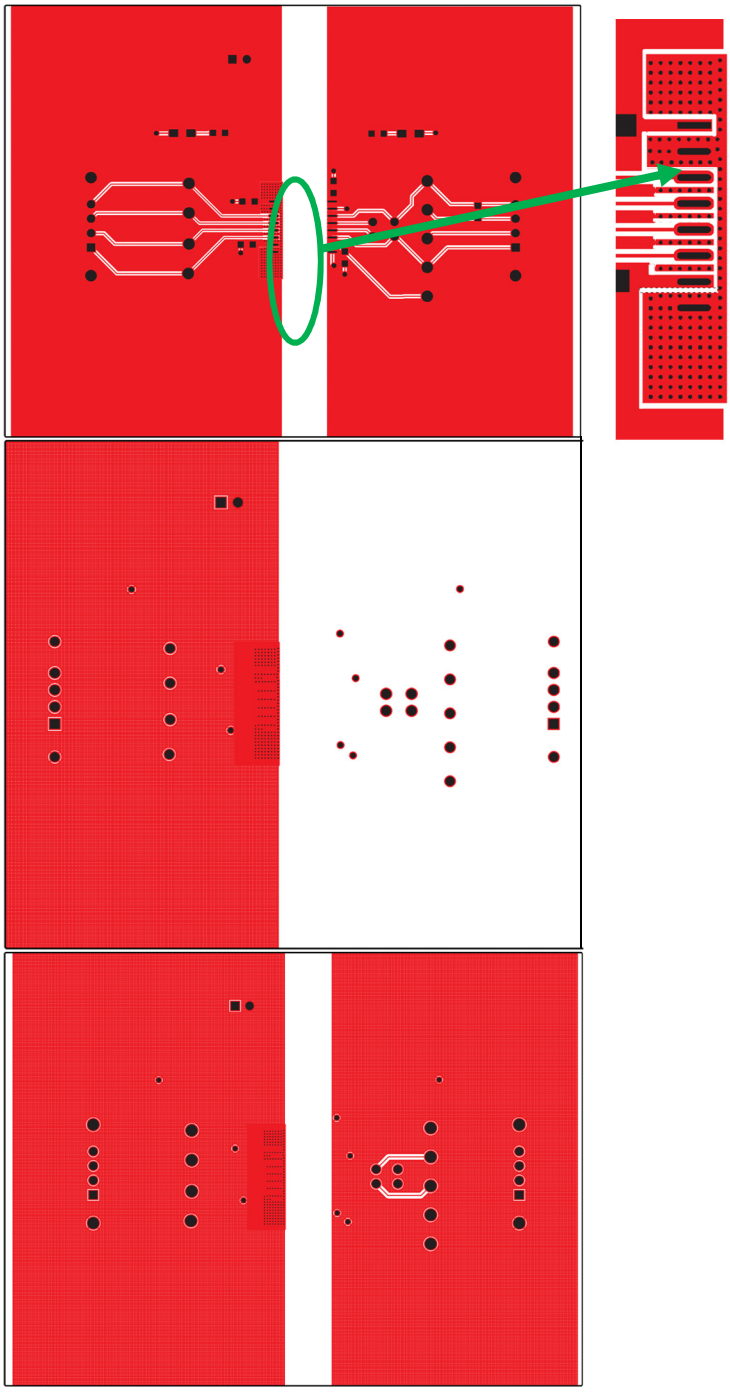

Figure 6. IL4622-01 Evaluation PCB Layout. Top left: top layer. Top right: controller side close-up. Middle: inner layers. Bottom: bottom layer.

Example: IL4622-01 Evaluation Boards

The IL4622-01 is a four-layer 2s2p-style board with a dense array of thermal vias in close proximity to the ground connection on the controller side.

The top layer is a mixed signal/power plane layer on both sides of the isolation barrier. Two inner layers have ground planes on the input side. The bottom layer is the ground plane layer on both sides of the isolation barrier.

The board has two-ounce copper outer layers and one-ounce copper inner layers. One-ounce copper outer layers can be used in some cases to save costs. Double sided boards in this configuration can be used, and two-ounce copper is recommended in these instances.

Designers do not need to allocate the entirety of the inner layers to an electrical ground-plane connection. For standard four-layer boards, it is recommended to allocate a certain fraction of each layer to thermal management. This can be limited to sections near the thermal via array on the device input side. A good rule-of thumb is to allocate one square-inch of copper for thermal spreading on each layer.

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To test the thermal techniques outlined in this bulletin yourself, check out our isolator evaluation kits, which are constantly re-stocked: www.nve.com/webstore/catalog/index.php?cPath=30_44

For a live demonstration of DC-DC converters and other isolator and sensor products, check out our *YouTube* channel: www.youtube.com/c/NveCorporation

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NVE Engineers are experts in thermal design and eager to help. Please contact iso-apps@nve.com for solutions to your thermal design problems.

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