Thermal Magnetic Random Access Memory

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New Memory Technologies

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James Deak

NVE Corporation

Participants

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- **Dave Brownell**
- **Pete Eames**
- **John Taylor**

Supported in part by DARPA

Motivation

MRAM combines the non-volatility and infinite endurance of magnetic based memories with silicon processing technology

	existing				emerging	
	SRAM	DRAM	Flash	FeRAM	CRAM	MRAM
Storage Mechanism	CMOS gates	charged capacitor	charge tunneling	ferroelectric capacitor	amorphous / crystalline resistivity	FM moment orientation
Read Speed	Fastest	Medium	Fast	Fast	Fast	Fast
Write Speed	Fastest	Medium	Slow	Fast	Medium	Fast
Endurance	Infinite	Infinite	1E5	>1E10	1E12	Infinite
Power	Low	High	Low	Low	Low	Low
Refresh	No	Yes	No	No	No	No
Potential Cell Density	Low	High	High	Medium	High	High
Non-volatility	No	No	Yes	Yes	Yes	Yes

Magnetoresistive Random Access Memory, By Saied Tehrani et al.

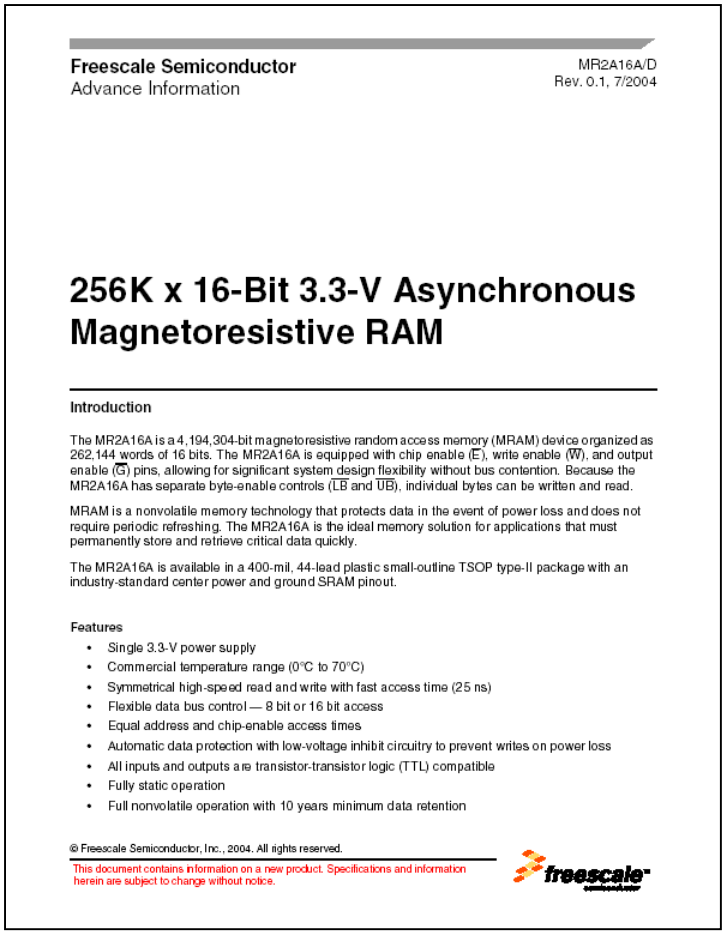
MRAM Issues:

- How to reliably select a random bit for writing
- How to combine low power and data retention

Outline

- MRAM Introduction
  - Status
  - MRAM Background
- MRAM Scaling Issues
- Magnetothermal MRAM
  - Modes – Curie, Neel/blocking temperature
  - Design Requirements
  - Thermal Writing Experiments
- Conclusions

MRAM Technology Status



Freescale Semiconductor
Advance Information

MR2A16A/D
Rev. 0.1, 7/2004

256K x 16-Bit 3.3-V Asynchronous Magnetoresistive RAM

Introduction

The MR2A16A is a 4,194,304-bit magnetoresistive random access memory (MRAM) device organized as 262,144 words of 16 bits. The MR2A16A is equipped with chip enable ($\overline{E}$), write enable ($\overline{W}$), and output enable ($\overline{G}$) pins, allowing for significant system design flexibility without bus contention. Because the MR2A16A has separate byte-enable controls ($\overline{LB}$ and $\overline{UB}$), individual bytes can be written and read.

MRAM is a nonvolatile memory technology that protects data in the event of power loss and does not require periodic refreshing. The MR2A16A is the ideal memory solution for applications that must permanently store and retrieve critical data quickly.

The MR2A16A is available in a 400-mil, 44-lead plastic small-outline TSOP type-II package with an industry-standard center power and ground SRAM pinout.

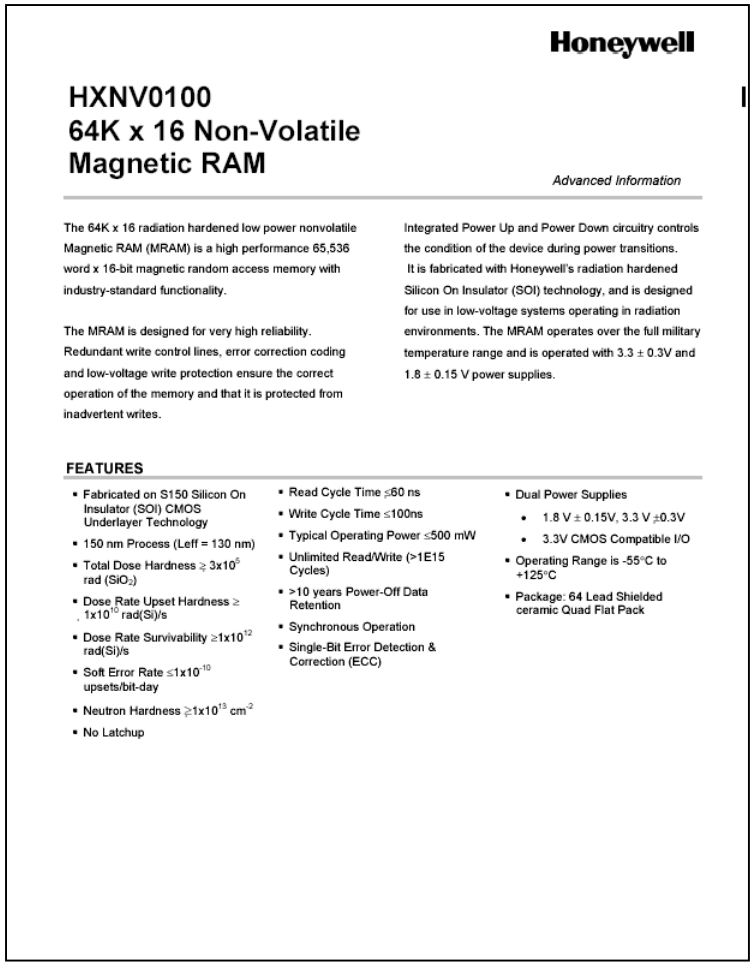
Features

- Single 3.3-V power supply
- Commercial temperature range (0°C to 70°C)
- Symmetrical high-speed read and write with fast access time (25 ns)
- Flexible data bus control — 8 bit or 16 bit access
- Equal address and chip-enable access times
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- All inputs and outputs are transistor-transistor logic (TTL) compatible
- Fully static operation
- Full nonvolatile operation with 10 years minimum data retention

This document contains information on a new product. Specifications and information herein are subject to change without notice.

freescale

Currently Sampling



Honeywell

HXNV0100
64K x 16 Non-Volatile Magnetic RAM

Advanced Information

The 64K x 16 radiation hardened low power nonvolatile Magnetic RAM (MRAM) is a high performance 65,536 word x 16-bit magnetic random access memory with industry-standard functionality.

The MRAM is designed for very high reliability. Redundant write control lines, error correction coding and low-voltage write protection ensure the correct operation of the memory and that it is protected from inadvertent writes.

Integrated Power Up and Power Down circuitry controls the condition of the device during power transitions. It is fabricated with Honeywell's radiation hardened Silicon On Insulator (SOI) technology, and is designed for use in low-voltage systems operating in radiation environments. The MRAM operates over the full military temperature range and is operated with 3.3 ± 0.3V and 1.8 ± 0.15 V power supplies.

FEATURES

- Fabricated on S150 Silicon On Insulator (SOI) CMOS Underlayer Technology
- 150 nm Process (Leff = 130 nm)
- Total Dose Hardness ≥ $3x10^5$ rad (SiO_2)
- Dose Rate Upset Hardness ≥ , $1x10^{10}$ rad(Si)/s
- Dose Rate Survivability ≥$1x10^{12}$ rad(Si)/s
- Soft Error Rate ≤$1x10^{-10}$ upsets/bit-day
- Neutron Hardness ≥$1x10^{13}$ cm^{-2}
- No Latchup
- Read Cycle Time ≤60 ns
- Write Cycle Time ≤100ns
- Typical Operating Power ≤500 mW
- Unlimited Read/Write (>1E15 Cycles)
- >10 years Power-Off Data Retention
- Synchronous Operation
- Single-Bit Error Detection & Correction (ECC)
- Dual Power Supplies
  - 1.8 V ± 0.15V, 3.3 V ±0.3V
  - 3.3V CMOS Compatible I/O
- Operating Range is -55°C to +125°C
- Package: 64 Lead Shielded ceramic Quad Flat Pack

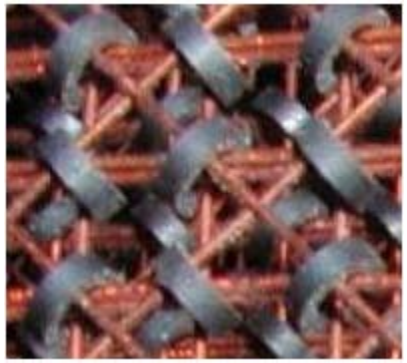
Expected 2006

NVE
NVE CORPORATION

Magnetic Memories

- Hard drives
- Tape drives
- Floppy disks
- Magnetic Core Memory – 1948 thru the 1970s

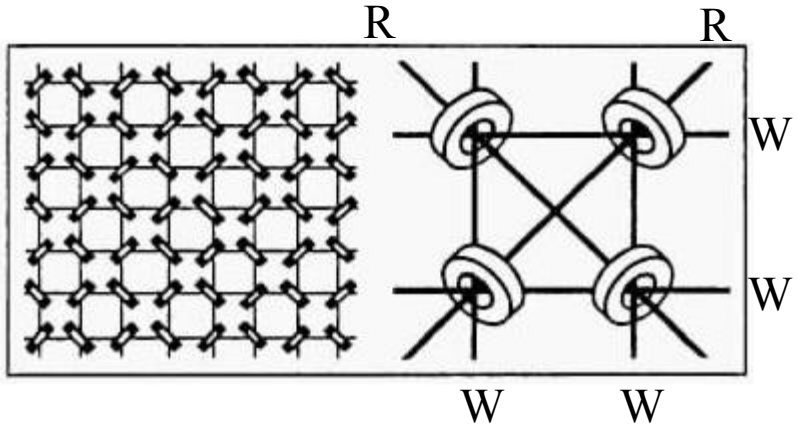
Core memory stack



53k bit in 512 cubic inches

http://www.fortunecity.com/marina/reach/435/coremem.htm

Inductive Read



Consider magnetic core memory

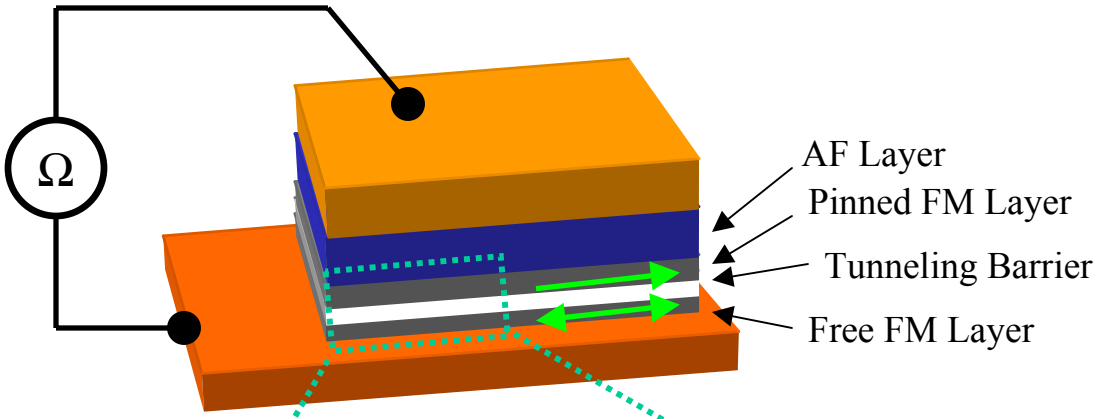
Here bits are read destructively by detecting a voltage pulse in a read line.

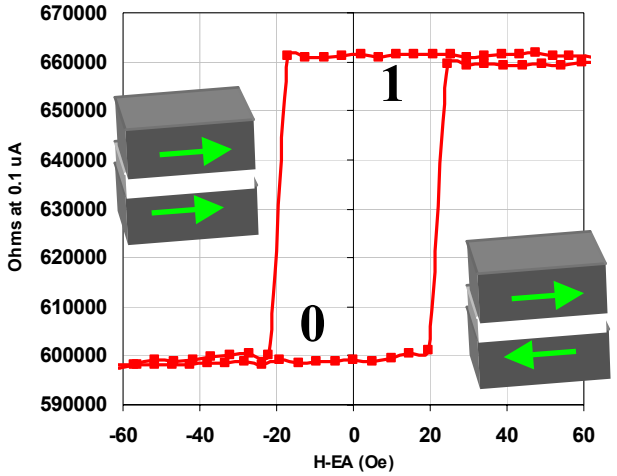
Voltage pulse created by writing a toroid at the intersection of two write conductors .

$$V_{sense} \propto (Volume)\frac{dM}{dt}$$

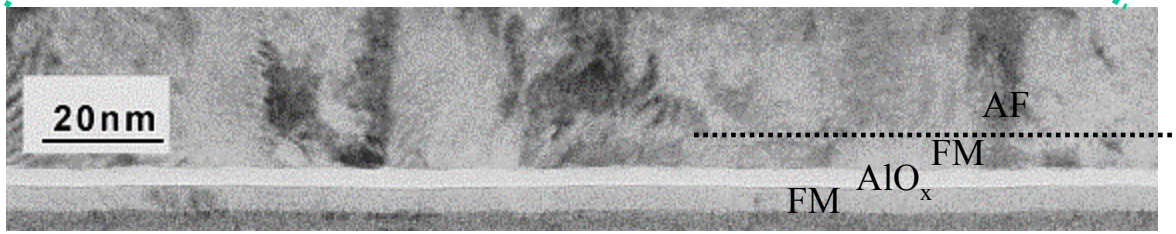
- Read signal decreases with decreasing magnetic bit size.
- Does not scale well.

Simple SDT Storage Element





TEM Cross-section of NVE SDT Barrier

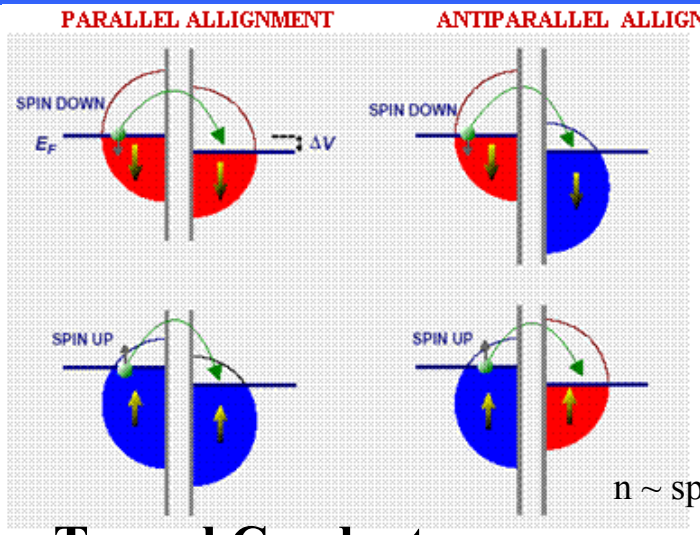


Tunneling Magnetoresistance

Julliere's Model

Phys. Lett. A 54, 225 (1975)

- Spin conserved during tunneling
- Two independent spin channels
- Parallel – Low Resistance
  - Majority→Majority
  - Minority→Minority
- Anti-Parallel – High Resistance
  - Majority→Minority
  - Minority→Majority
- Room Temperature Max. TMR
  - AlO_x ~ 70%
  - MgO ~ 260%



n ~ spin dependent DOS

Tunnel Conductance

$$G_{\uparrow\uparrow} \propto n_L^{\uparrow} n_R^{\uparrow} + n_L^{\downarrow} n_R^{\downarrow}$$ Parallel

$$G_{\uparrow\downarrow} \propto n_L^{\uparrow} n_R^{\downarrow} + n_L^{\downarrow} n_R^{\uparrow}$$ Anti-parallel

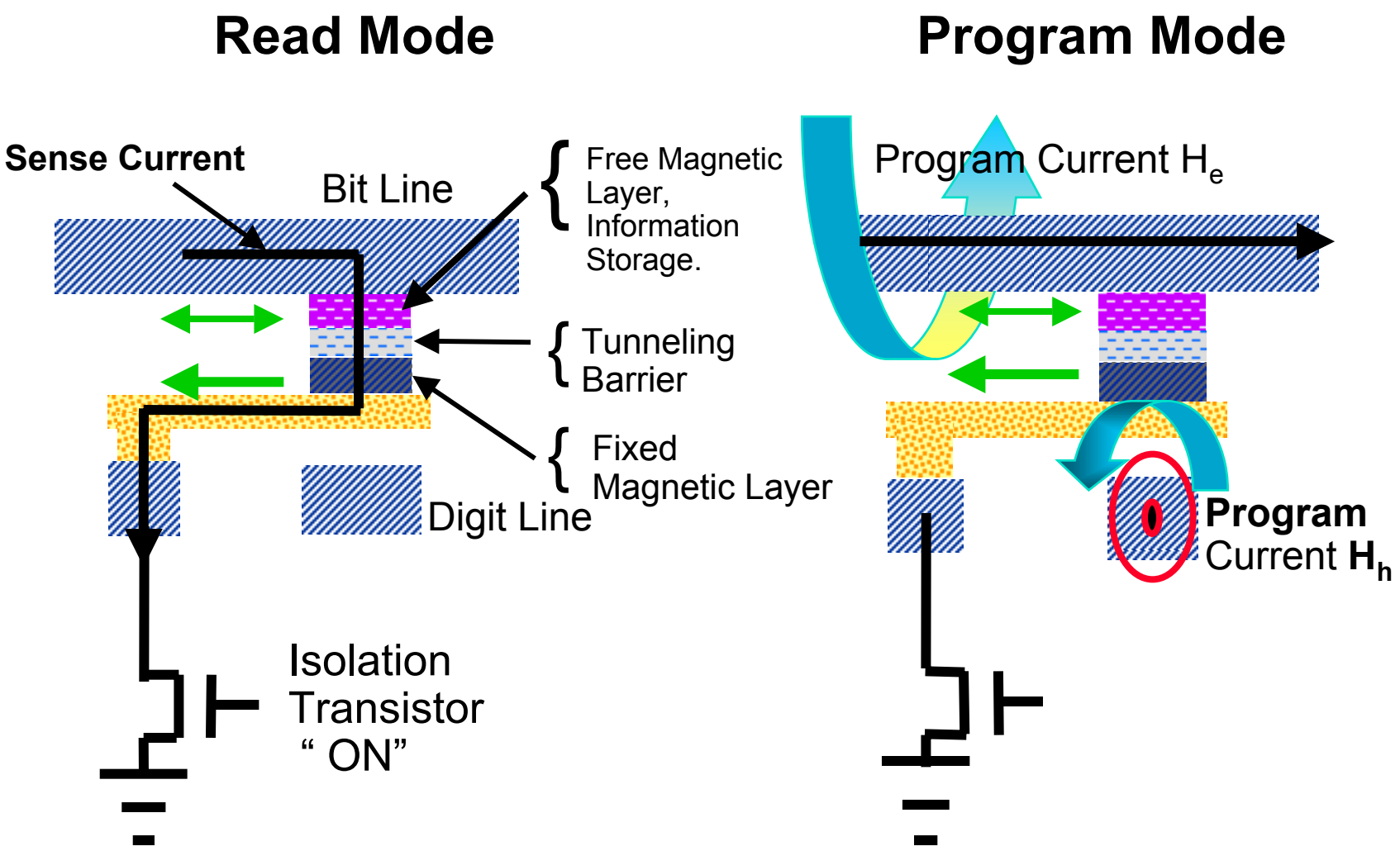
Magnetoresistance

$$TMR = \frac{G_{\uparrow\uparrow} - G_{\uparrow\downarrow}}{G_{\uparrow\downarrow}} = \frac{R_{AP} - R_P}{R_P} = \frac{2P_L P_R}{1 - P_L P_R}$$

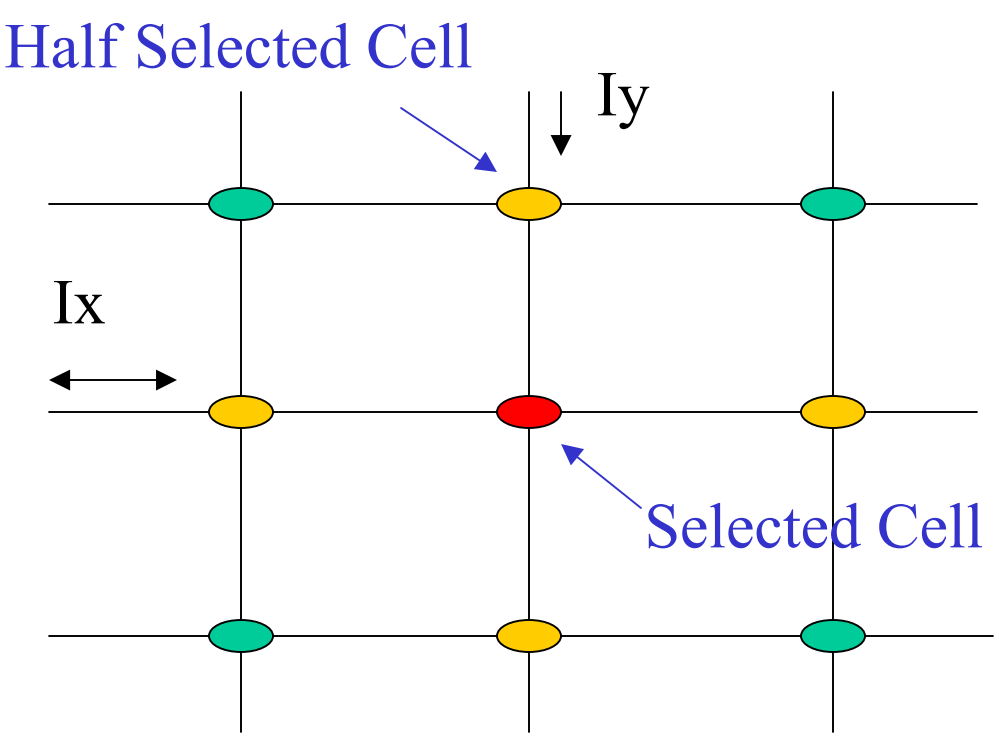
Spin Polarization

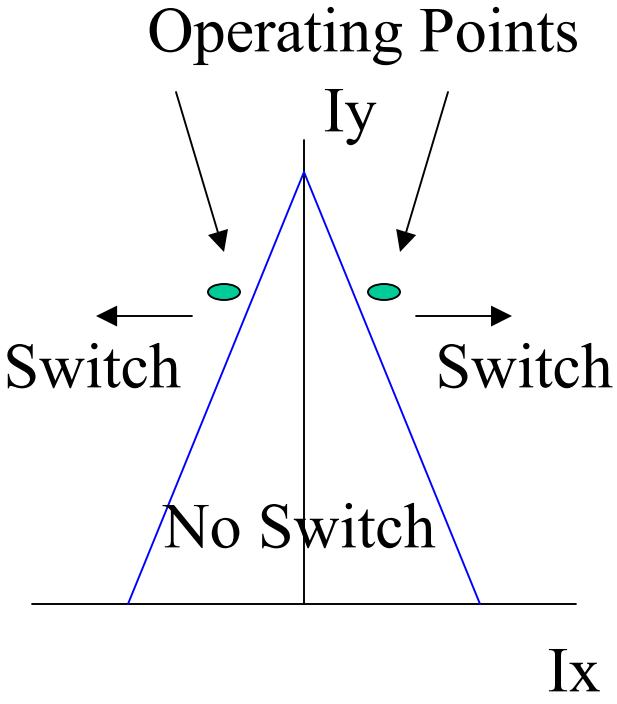
$$P_L = \frac{n_L^{\uparrow} - n_L^{\downarrow}}{n_L^{\uparrow} + n_L^{\downarrow}}$$ Left $$P_R = \frac{n_R^{\uparrow} - n_R^{\downarrow}}{n_R^{\uparrow} + n_R^{\downarrow}}$$ Right

Typical MRAM Cell



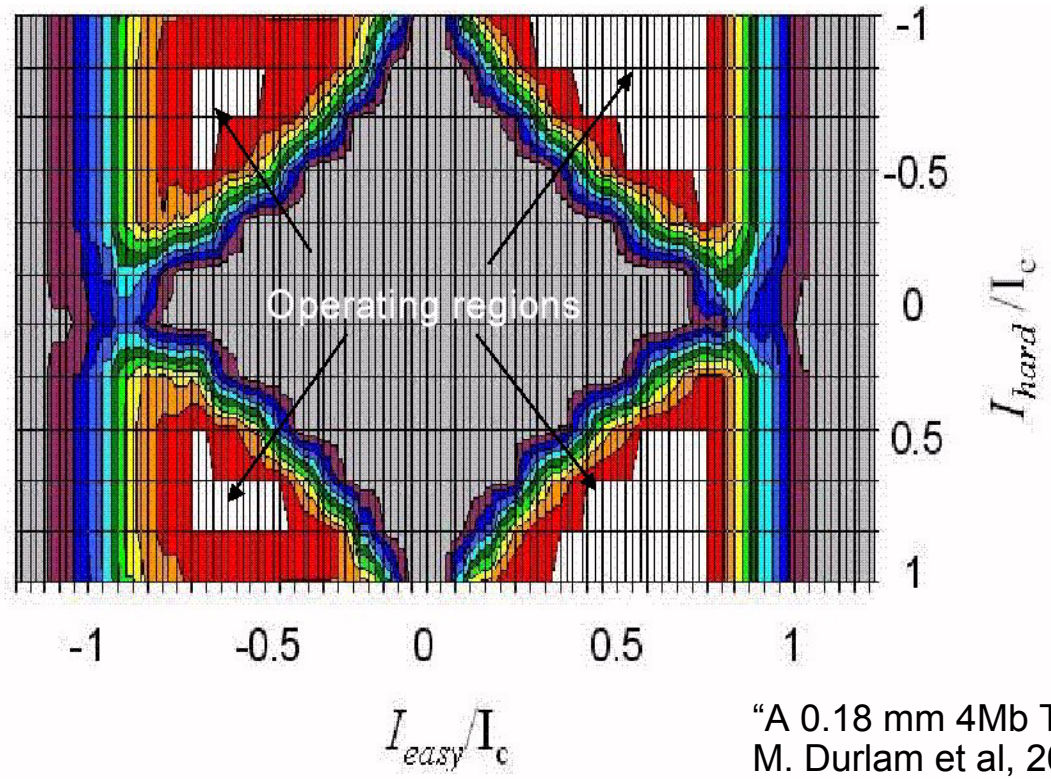
Stoner-Wohlfarth Write Select

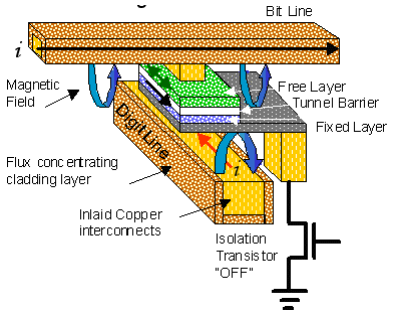




- Ix, Iy Alone Doesn't Switch Cell
- Ix, Iy Together Switch Cell

Margins With Old Cell - Motorola





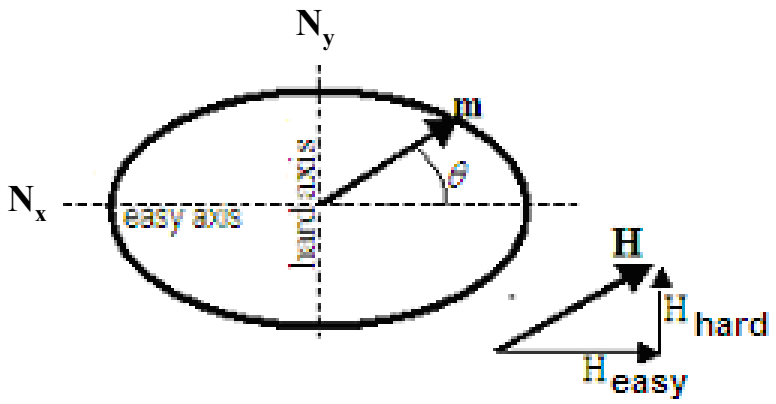
"A 0.18 mm 4Mb Toggling MRAM",
M. Durlam et al, 2003 IEEE Publication

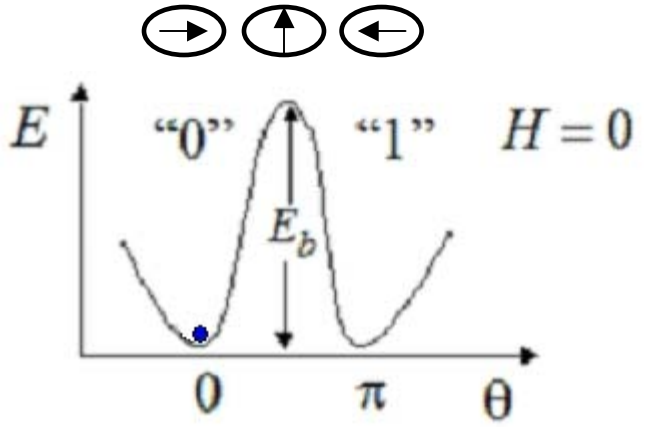
Control of the distribution of switching fields makes the SW-MRAM implementation difficult to manufacture and scale.

Becomes more difficult as cell size is reduced

Stability and Thermal Activation

Magnetic Energy





$$E = -\frac{1}{2}(N_y - N_x)M_s^2 V \sin^2\theta - M_s\left(H_{easy}\cos\theta + H_{hard}\sin\theta\right)V$$

$$E_b = \frac{1}{2}(N_y - N_x)M_s^2 V = KV$$

$$H_c = 2K / M_s$$

Probability for magnetization to be reversed by thermal activation in time t is

$$P(t) = 1 - \exp(-t/\tau) \qquad \text{where} \qquad \frac{1}{\tau} = f_0 \exp\left(\frac{-E_b(H)}{k_B T}\right)$$

Increasing E_b/k_BT increases the retention time but also increases programming field

Energy Barrier and Error Rate in MRAM

Error Rate is related to the Barrier Height

$$P(t) = \frac{N_{rev}}{N_{bits}} = 1 - e^{-t/\tau} = 1 - e^{-tf_0 e^{-E_b/k_B T}}$$

$$-tf_0 e^{-E_b/k_B T} = \ln\left\{1 - \frac{N_{rev}}{N_{bits}}\right\} \approx -\frac{N_{rev}}{N_{bits}} \qquad \text{If } N_{rev} << N_{bits}$$

$$\frac{N_{rev}}{t} = \frac{err}{s} = N_{bits} f_0 e^{-E_b/k_B T}$$

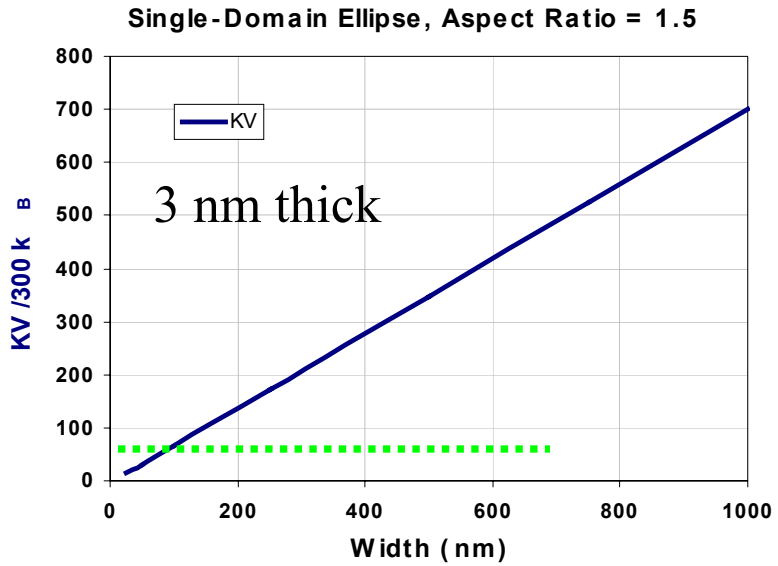
$$\frac{err}{hr} = (WritFrac) N_{bits} f_0 e^{\frac{-E_b(H)}{k_B T}} \left(3600 \frac{s}{hr}\right)$$

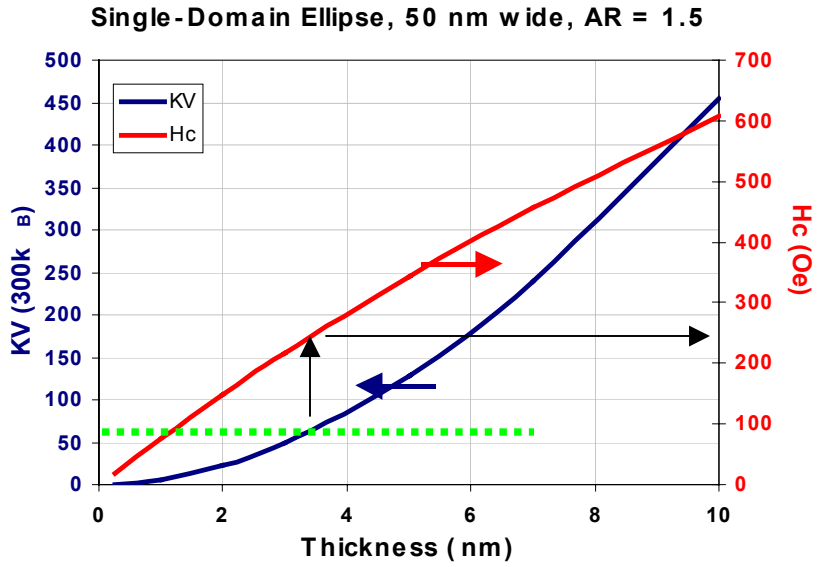
Energy barrier can thus be determined as

$$E_b = -\ln\left[\frac{err/hr}{(WrtFrac)(N)(f_0)(3600)}\right] k_B T$$

- Required E_b is thus directly related to the desired error rate , T, and N_{bits}
- E_b should be > 66 $k_B T$ ~ 3.7e-19 J, for 1 Mbit, 1e-10 err/hr, 400 K

Write Current and Cell Size





- Small volume lowers thermal stability – need to increase thickness with decreasing size

- For small single layer free layers, increasing stability increases write field/current to impractical values

MRAM Scaling Issues

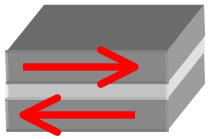
- **Control of switching field distributions**
- **Large write current required for stability**

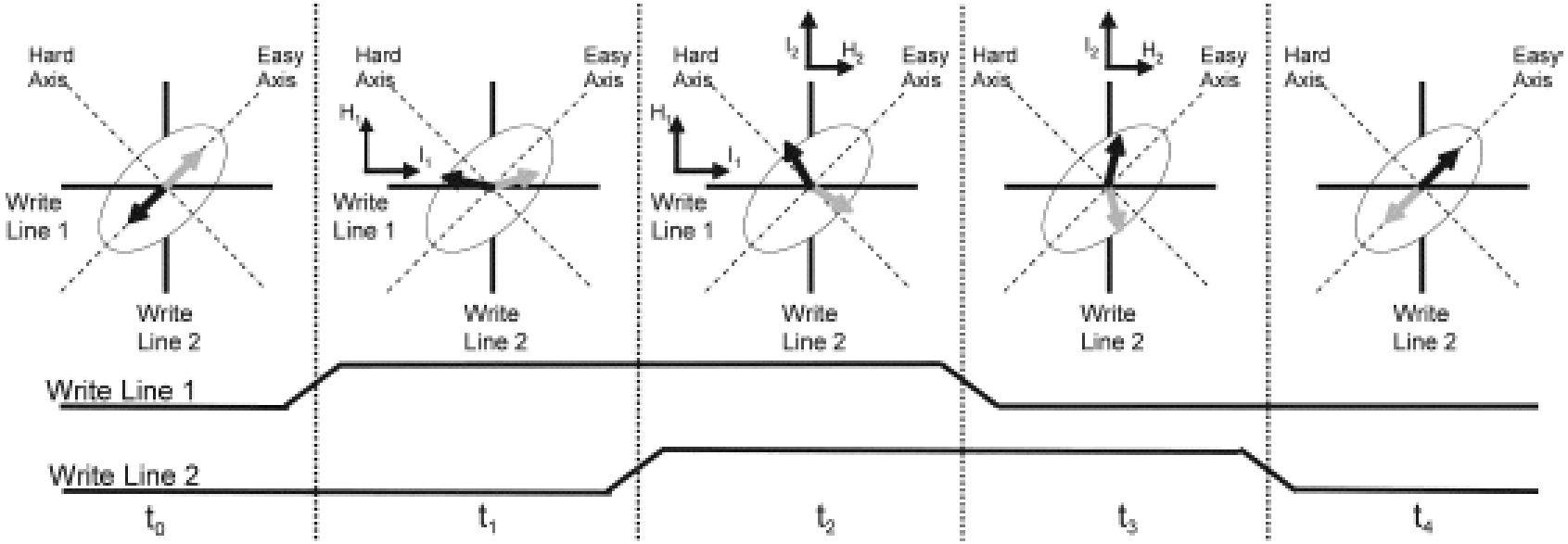
Alternative Write Methods

- Toggle
- Spin Momentum Transfer
- Thermal Writing
  - –Curie Point Write, T_c
  - –Neel (T_N) or Blocking Temperature (T_B) Write
  - –Thermal Spin-Momentum Transfer Write, T-SMT

Savtchenko "Toggle" Write

- Enhanced write selectivity due to pulse sequence
- SAF Stack FM/Ru/FM

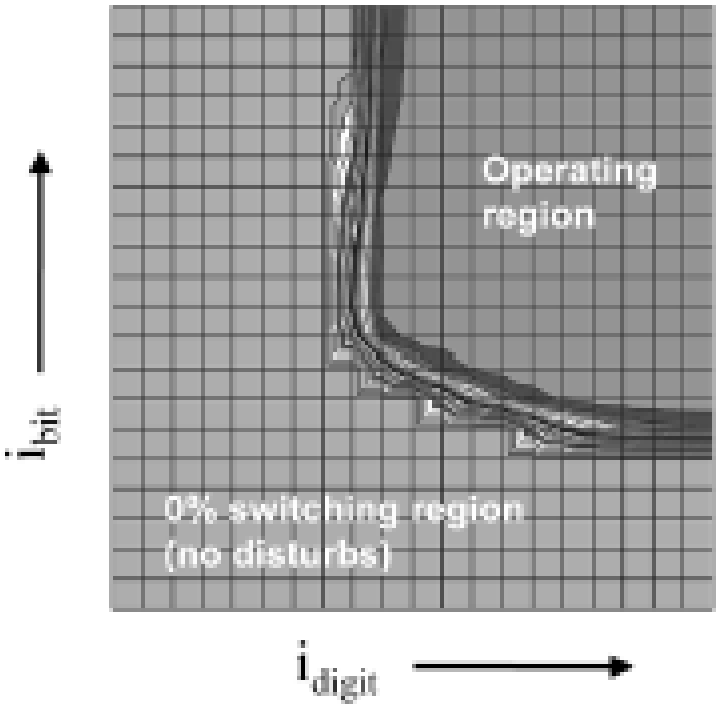




Toggle Switching Mode

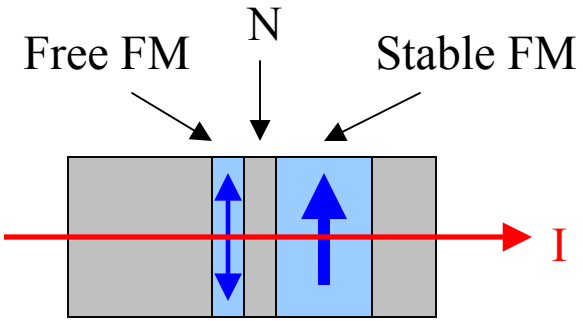
Freescale 4 Mbit MRAM
- CMOS 0.18 µm
- 1T/1MTJ
- 25 ns Write/read
- 48 F^2 cell (1.55 μm^2)

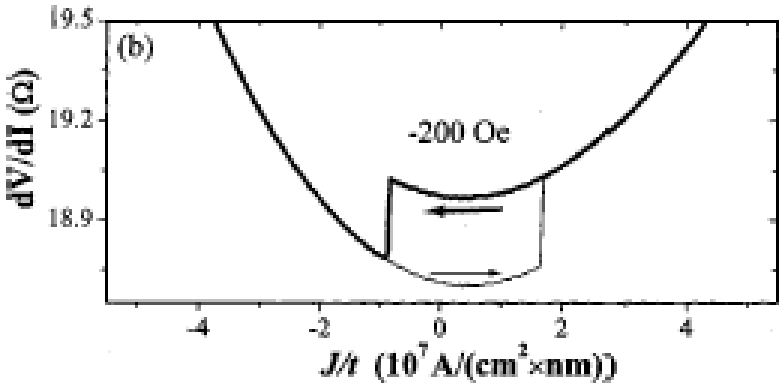
Results
- Excellent Selectivity
- High write current (~7 mA/line)

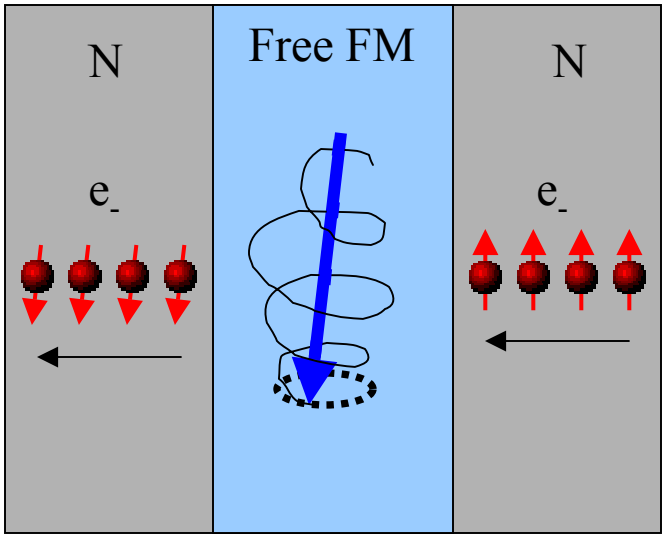


Thermal stability at small bit size still an issue → high write current

SMT Switching – Basic Picture







- No external field required to reverse magnetization
- Angular momentum exchange between spin polarized current and ferromagnet induces torque and precession
  Torque ~ $\pm J\, \boldsymbol{M}_2 \times (\boldsymbol{M}_1 \times \boldsymbol{M}_2)$; $J \sim 10^7$ A/cm2
  Slonczewski (1996)
- At critical I precession large and magnetization precesses into reversed state
- Reversed magnetization stable since torque becomes zero

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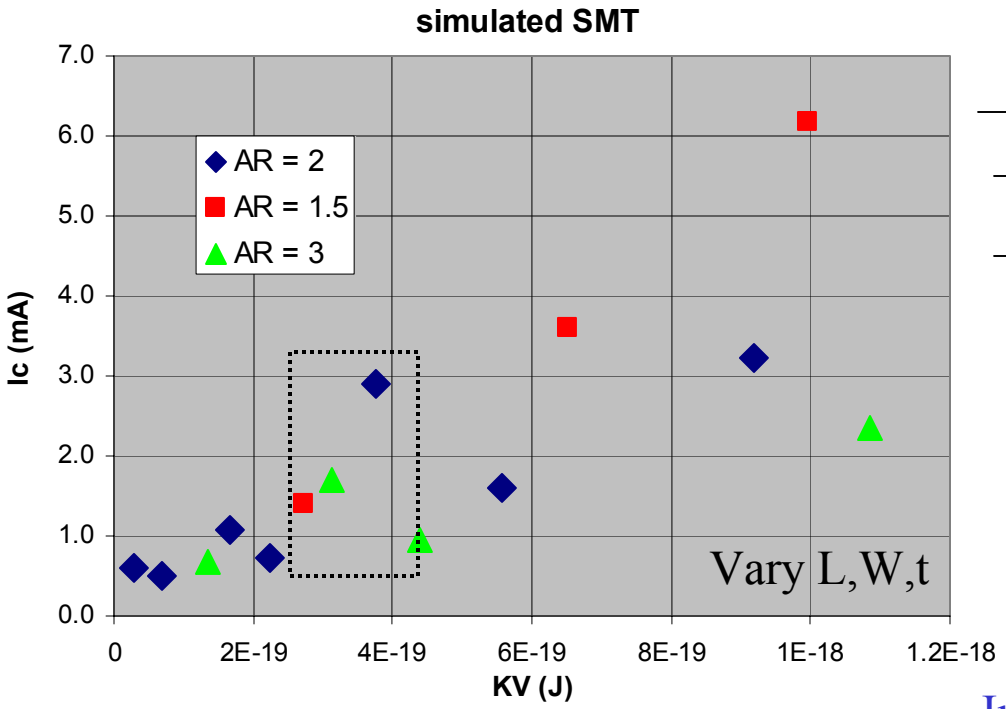
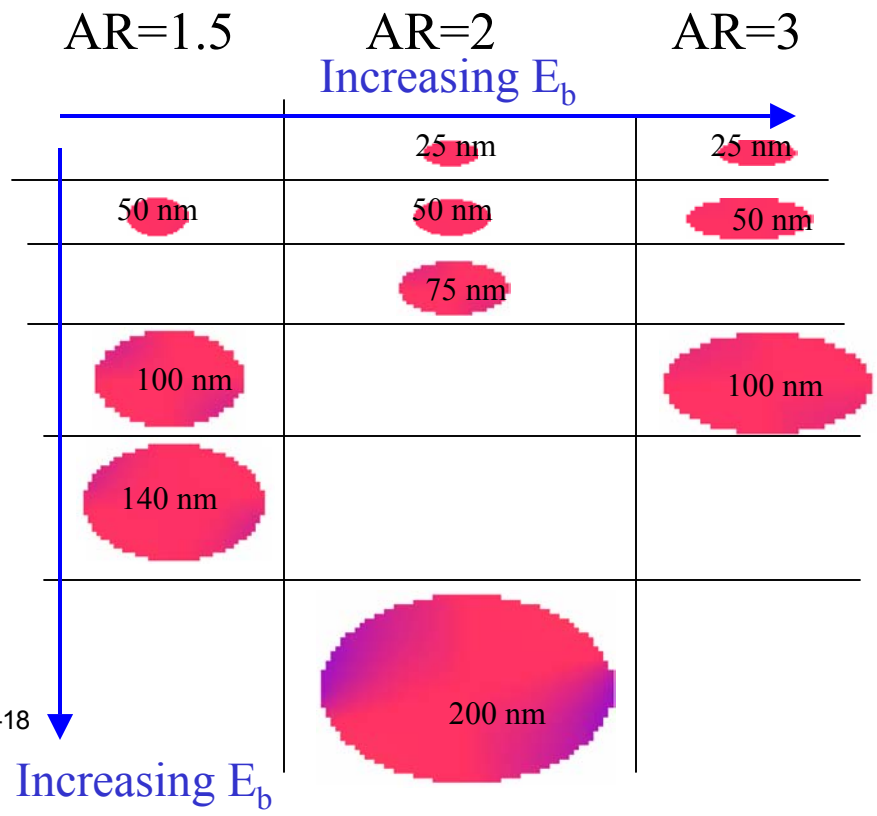
SMT I_c vs. E_b





E_b must remain high as bit size is scaled down – thickness must increase

Switching roughly proportional to E_b

At fixed E_b, smaller AR bits require more current

Smaller dimensions do not guarantee lower write current!

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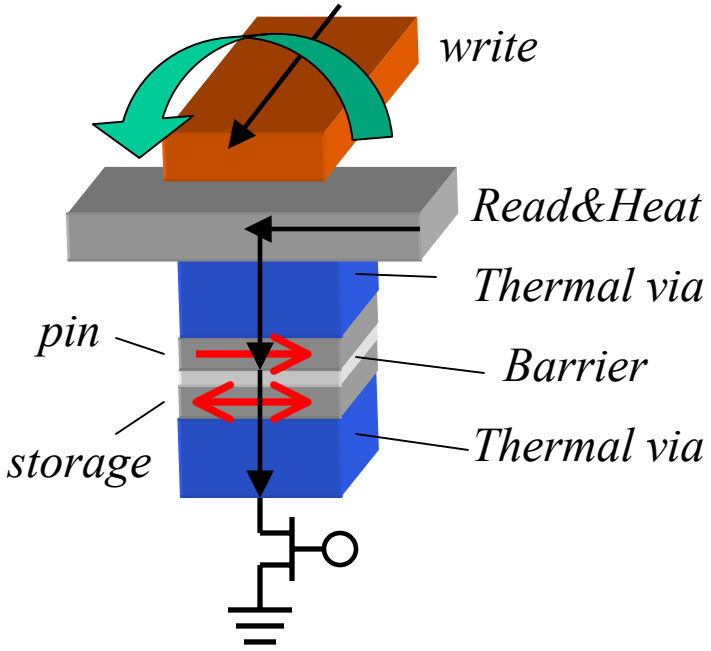
Magnetothermal MRAM

Principle of operation

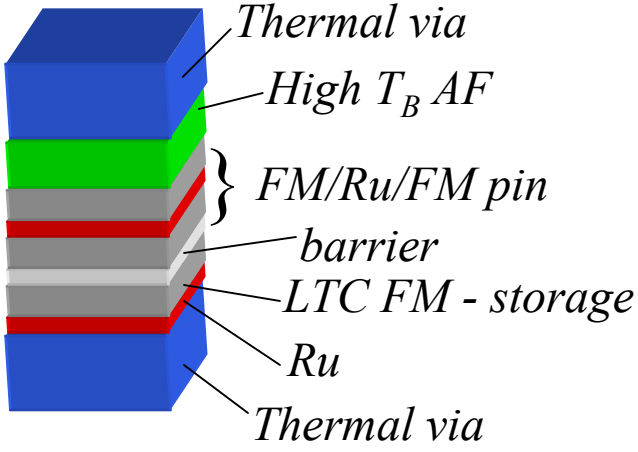
- Use a very high stability storage layer to improve data retention.
- Apply current through the tunnel junction to heat the storage layer
- Storage layer coercivity reduced at high temperature
- Storage layer may be an AF/FM bilayer or a low T_c FM



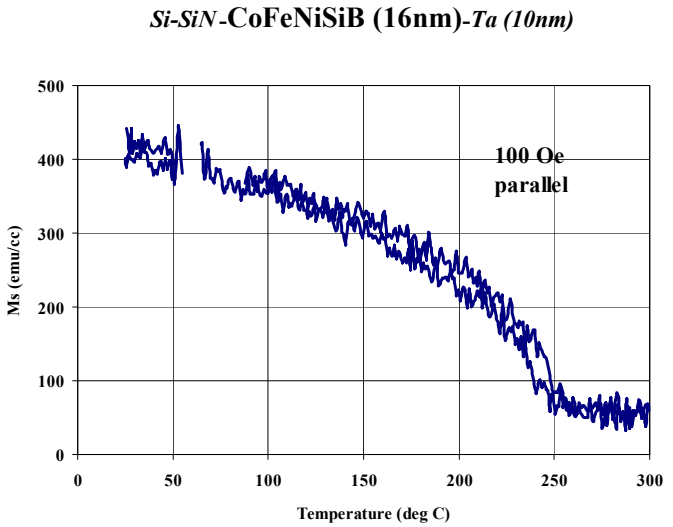
Goal: Design for high density →Heating current below 100 μA at 100 nm bit size

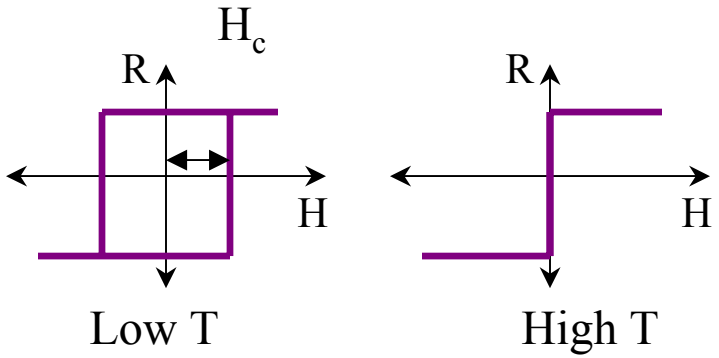
Curie Point MRAM

Curie



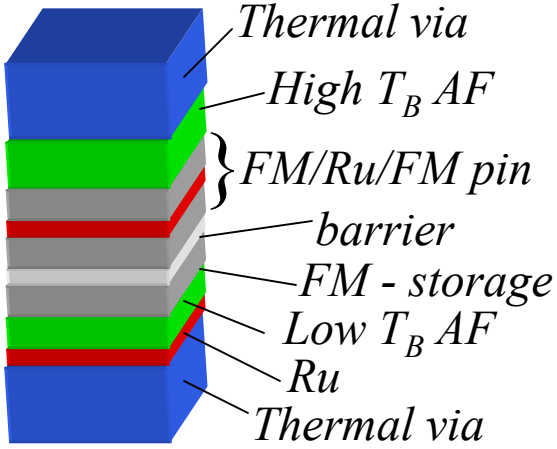
Coercivity drops due to reduction of free layer magnetization



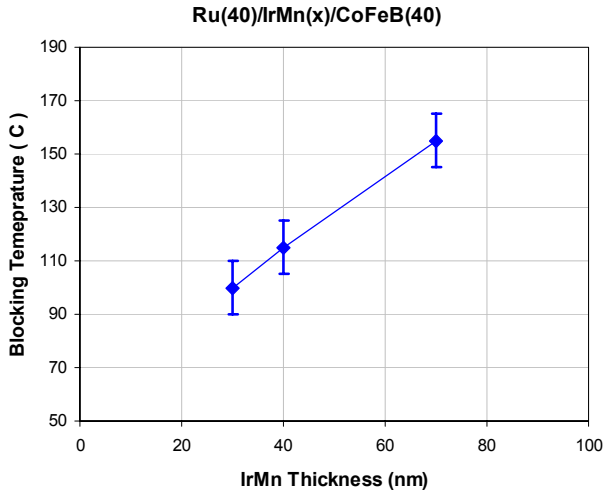


Neel Point MRAM

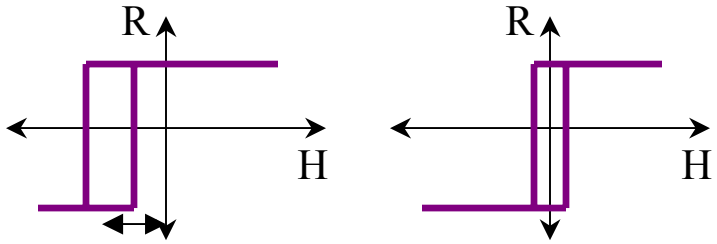
Neel or T_B



Offset field (H_{ex}) drops to zero at high temperature (T_B)



Best mode since AF/FM bilayer **easy to achieve high E_B** due to high FM/AF coupling and high AF anisotropy. Also has the **best magnetic field immunity.**



Low T High T

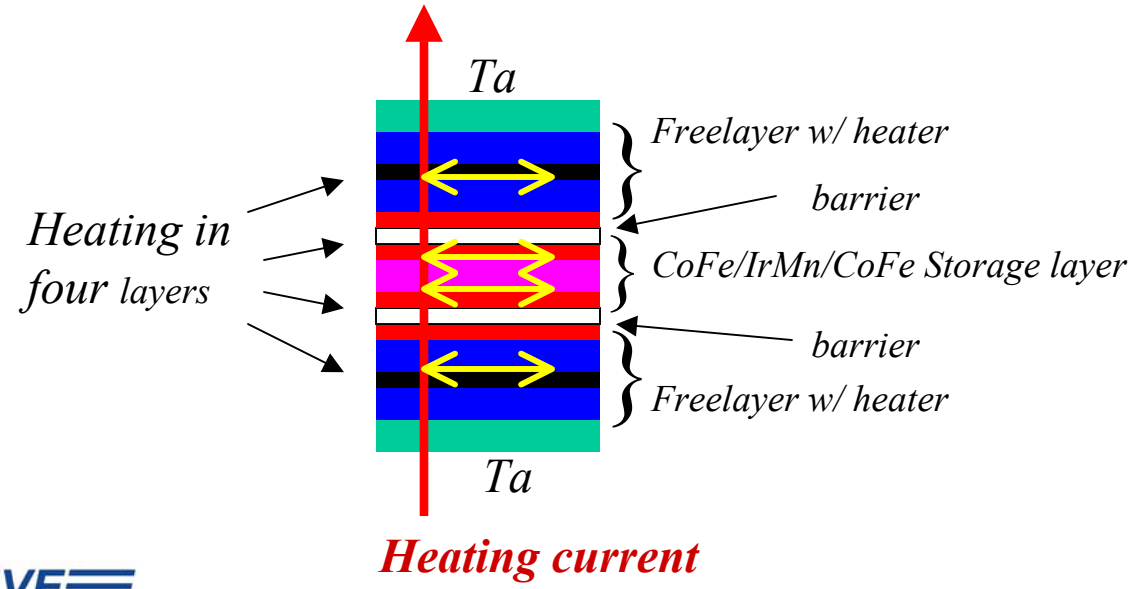
Previous T_B MRAM Work

2622 IEEE TRANSACTIONS ON MAGNETICS, VOL. 40, NO. 4, JULY 2004

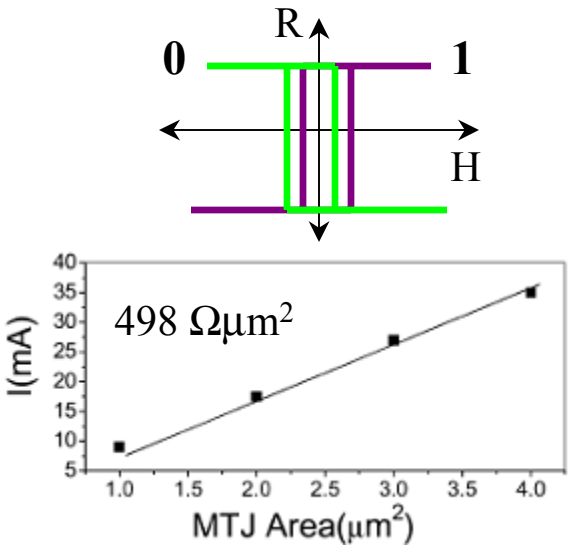
Low-Current Blocking Temperature Writing of Double-Barrier MRAM Cells

Jianguo Wang and P. P. Freitas

- **Heating through barrier confirmed**
- **T_B writing mechanism verified w/ 10 ns write pulse**
- **NOL layers used to increase RA and take stress off the barrier – at the expense of TMR – V_{lim} = 2 V**
- **Not expected to scale well due to stray field interaction in the FM/AF/FM storage layer**
- **Demonstrated >10^{10} thermal writes**



Digital value determined by freelayer R(H)



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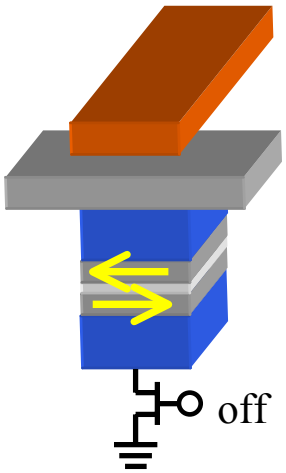
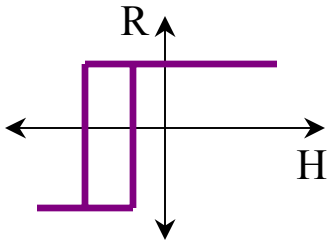
NVE Neel Point (or T_B) MRAM Operation

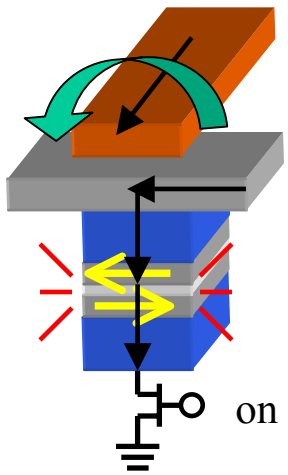
Write Sequence



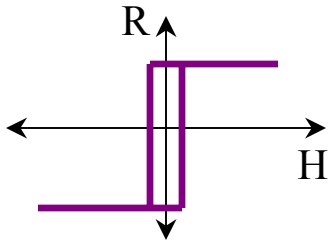
initial state: 1



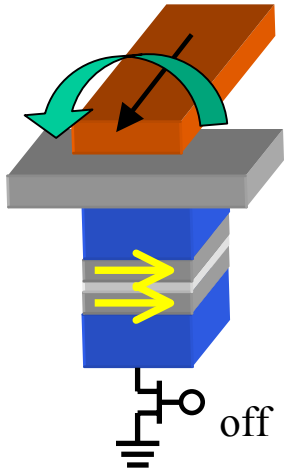
Apply heating and write currents



heat

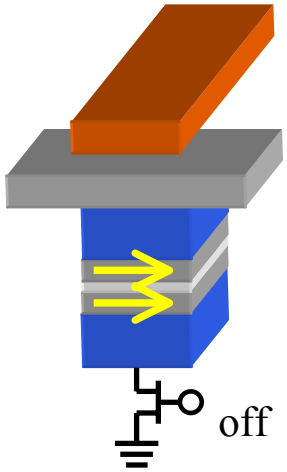


Turn off heating current

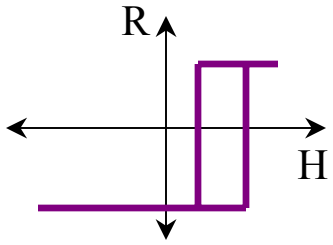


field cool

Turn off write current



final state: 0

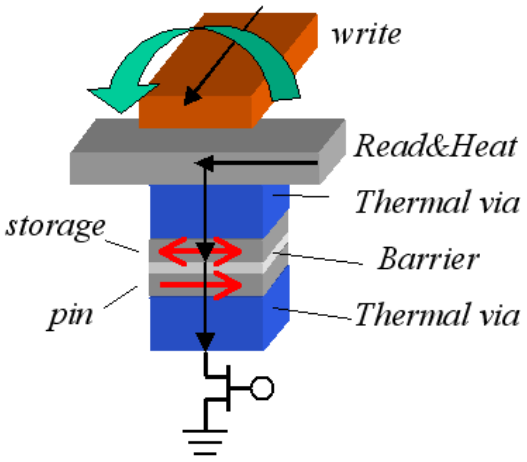


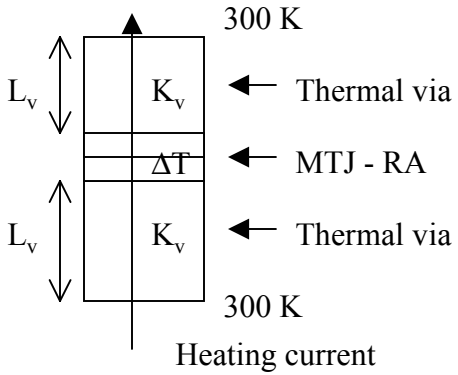
NVE CORPORATION

Neel Point MRAM Considerations

- Need margin between high T_b and Low T_b layers (Easy)
- Low thermal conductivity vias to lower write current (several alternative materials such as PtMn and BiTe)
- Low thermal conductivity encapsulating material to lower write current (process requires some work)
- Barrier RA must be optimized to permit efficient heating at low write current, while maintaining a large TMR (Not too easy, but not impossible)
- AF must have $H_{ex} > H_c$, Low H_c at T_B, $T_B > 150$ C (Easy)

Resistance Area Product Requirements





$P = I^2R$ – power

R – junction resistance

A – junction area

$\langle RA \rangle = \rho t$ – Junction resistance area product

K_v – via thermal conductivity

L_v – via length

I – heating current

$R_{th} = L_v/(2K_vA)$ – thermal resistance from barrier to 300 K heat sink

Junction temperature: $$\Delta T = R_{th}P = \frac{L_v}{2K_vA} I^2 \frac{\langle RA \rangle}{A}$$

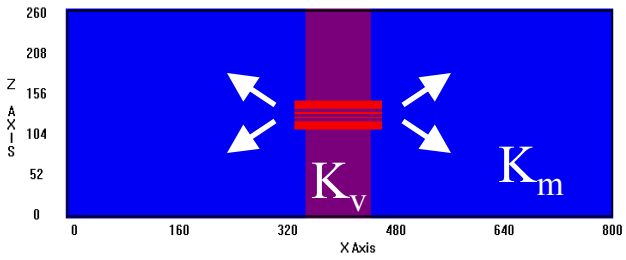
Heating current: $$I(\Delta T) = A\sqrt{\frac{\Delta T 2K_v}{L_v \langle RA \rangle}}$$ **Heating current proportional to bit area**

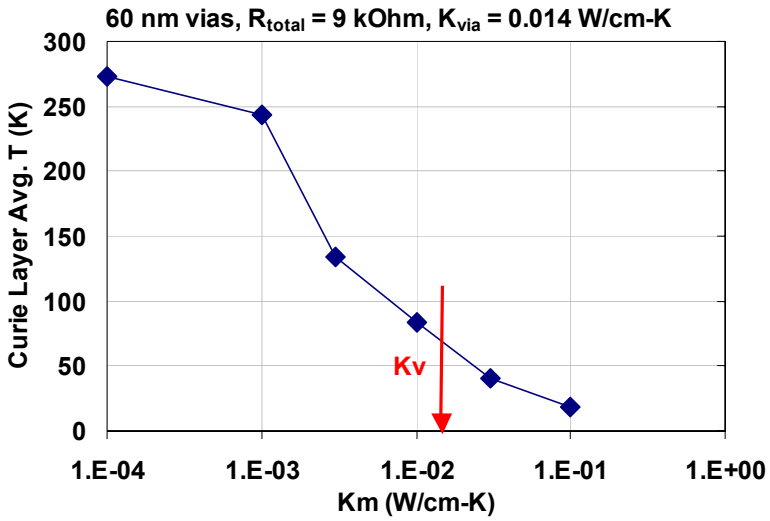
Voltage: $$V(\Delta T) = I(\Delta T)R = \sqrt{\frac{\Delta T 2K_v \langle RA \rangle}{L_v}}$$ **Must limit < ~0.5 V for reliability**

Maximum RA: $$\langle RA \rangle_{max} \leq \frac{V_{Lim}^2 L_v}{2\Delta T K_v}$$ **Optimal value depends on V_{lim}, R_{th}, and desired ΔT.**

NVE CORPORATION

Encapsulating Material Optimization

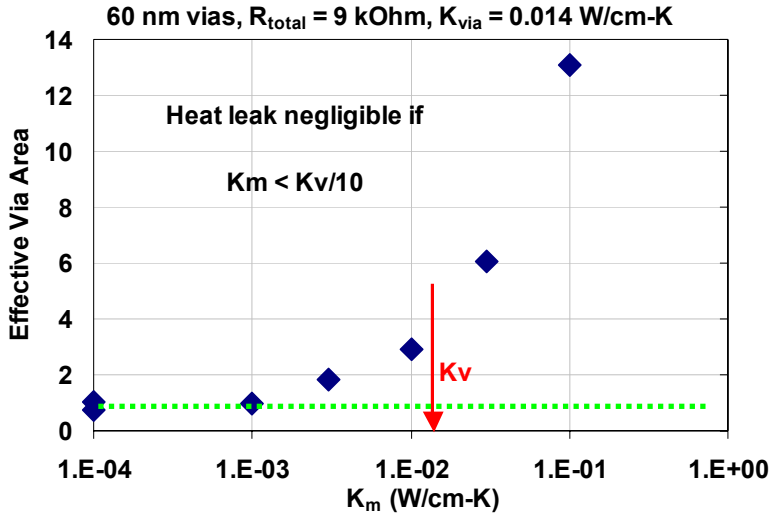




- Heat diffuses into the encapsulating material
→ Lowers heating efficiency

- Looks as if the thermal vias have a larger effective area

$$A_{eff} = \left(\frac{2K_v \Delta T}{PL}\right)\frac{1}{A_{via}}$$



Best if $K_m < K_v/10$

Thermal Via Optimization

$$\frac{K_v}{L_v} \leq \frac{V_{Lim}^2}{2\Delta T \langle RA \rangle_{max}}$$

- Need minimum K_v and large L_v
- Can't increase L_v too much
  - –Thermal rise time becomes too long
  - –Roughness becomes too large for low RA barrier
- Settle on 50 nm of PtMn
  - low K_v = 0.01 to 0.014 W/cm-K
  - Able to fabricate low RA junctions at this thickness

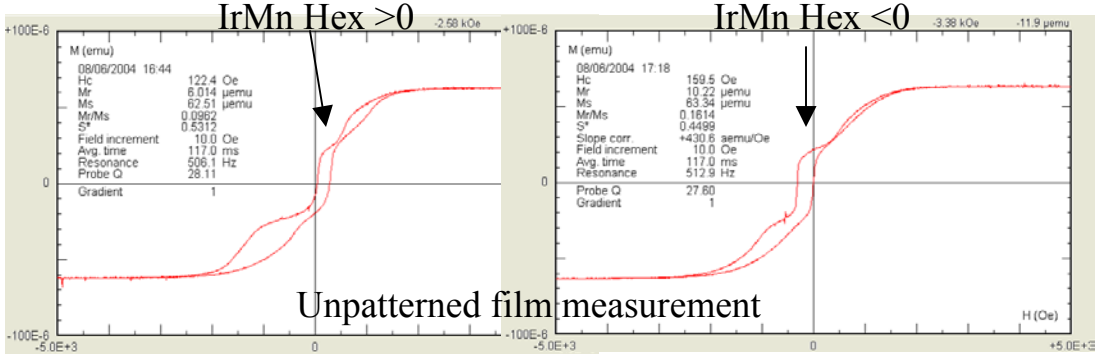
Test Structure Fabrication

Anneal Low T_b AF +H

IrMn Hex >0

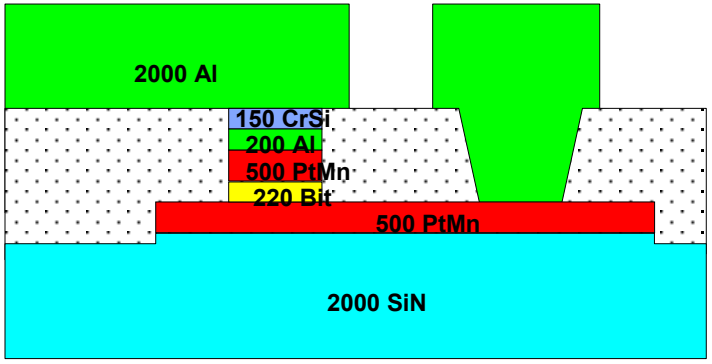
Anneal Low T_b AF -H

IrMn Hex <0

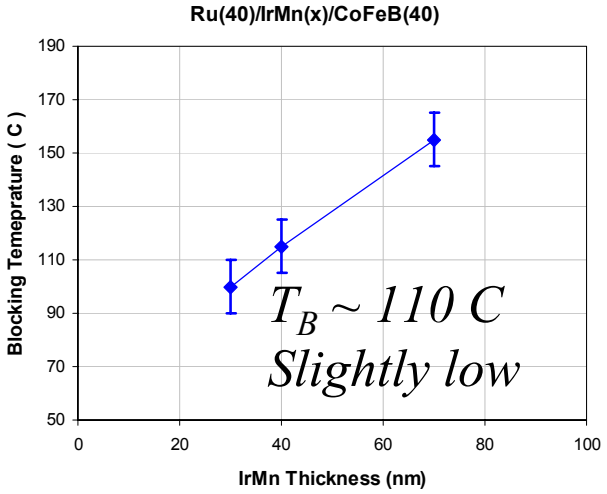


Unpatterned film measurement

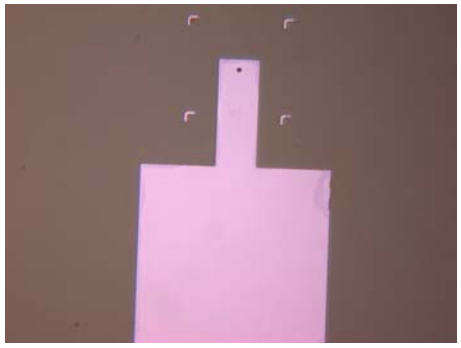
E-beam and optical lithography



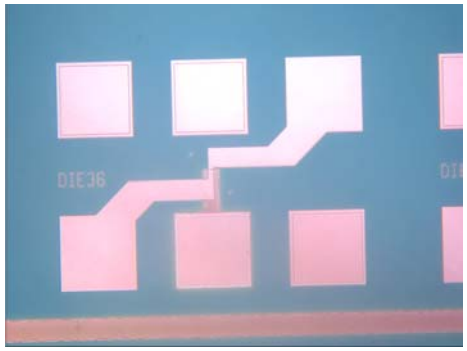
PtMn(50)/Ru(4)/IrMn(4)/CoFeB(4)/AlOx(x)/CoFeB(4)/Ru(0.7)/FeCo(4)/PtMn(50)/Al(20)



Bits patterned from 0.05 µm to 5 µm.



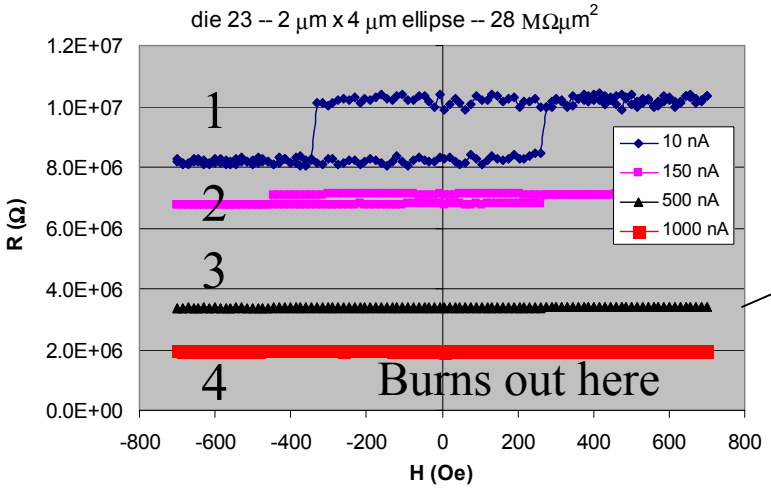
Post bit ion mill



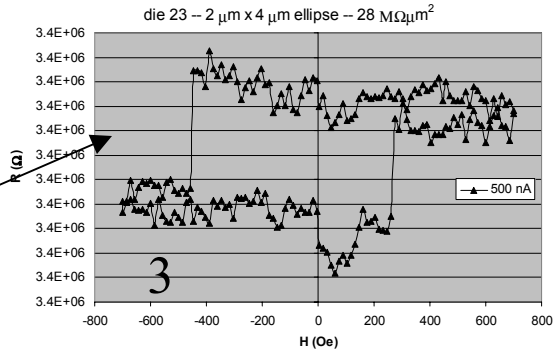
Post top conductor etch

Writing accomplished using external field

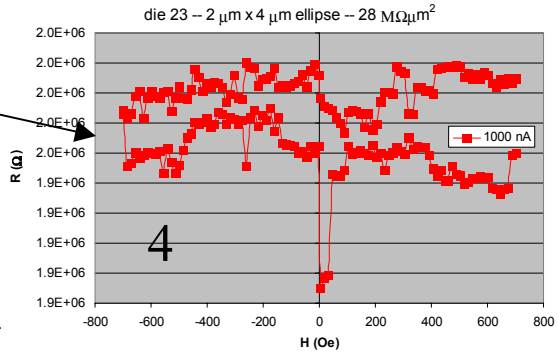
High RA Junction (13 Å Al, 28 MΩμm²)

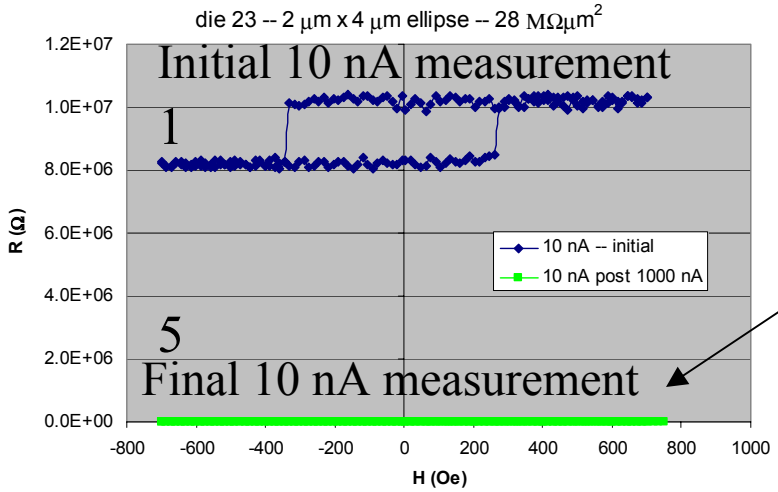


no change at 500 nA



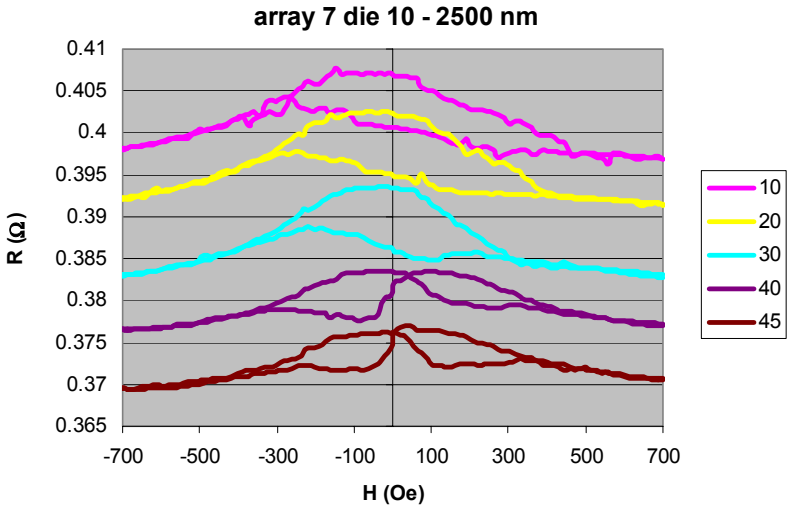
No TMR at 1000 nA
Check R(H) at lower current

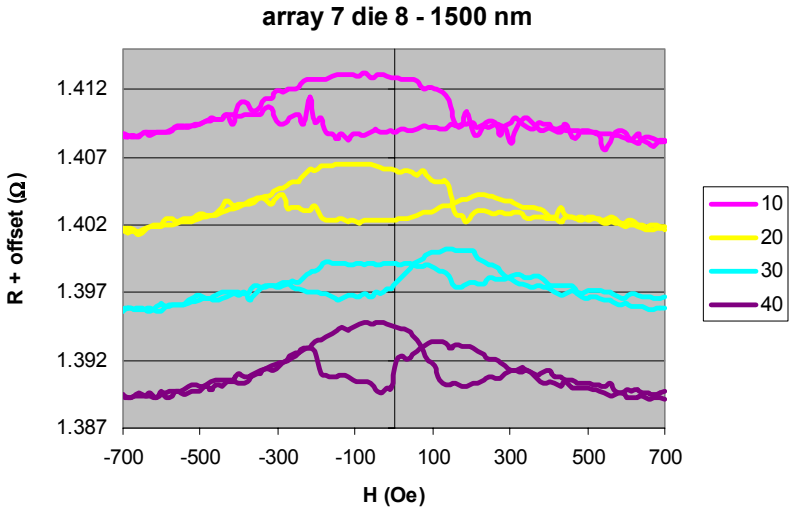


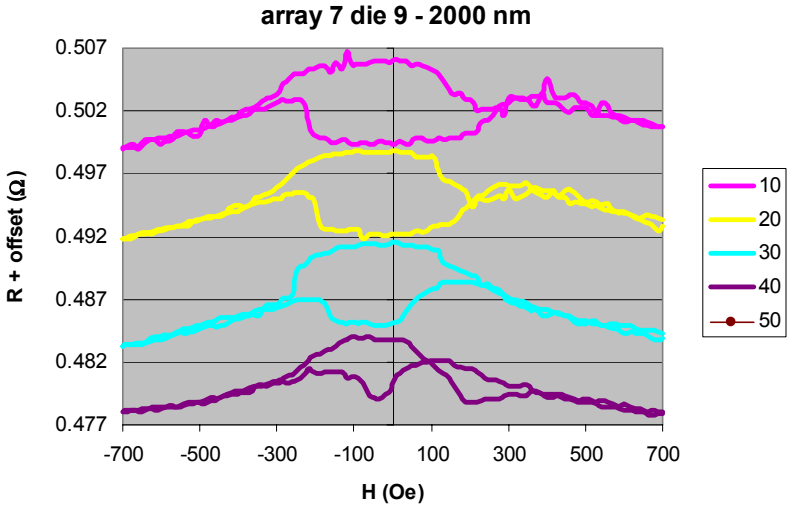


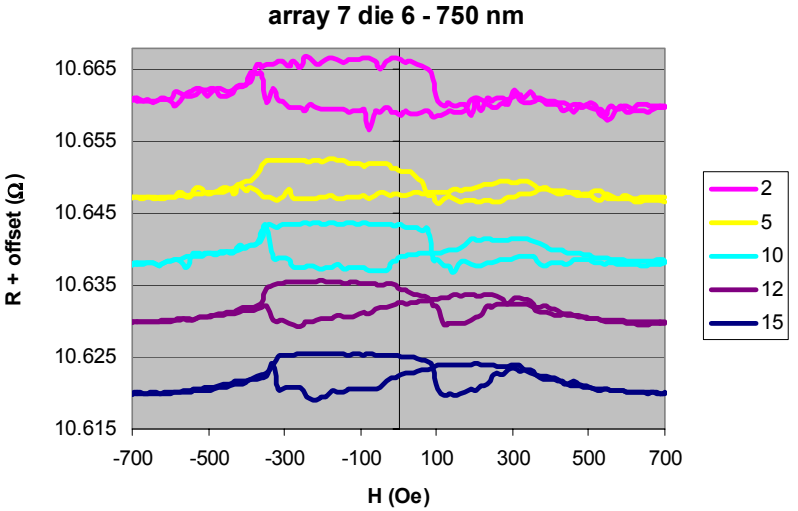
Device burns out before IrMn T_b is exceeded

Low RA Junction (6 Å Al, 5 Ωμm^2)









Changes from SV to PSV behavior – Why?

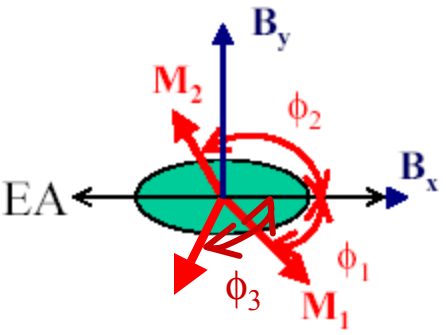
NVE CORPORATION

Model Description

Pinned layer/barrier/storage layer

$FM_1(t_1,M_{s1},K_1)/Ru(J_{RU})/FM_2(t_2,M_{s2},K_2)/AlO_x(J_{AlO})/FM_3(t_3,M_{s3},K_3)$

Strong coupling Weak coupling



Total Energy

$$E_{tot} = E_z + E_{exc} + E_K + E_d$$

External Fields

$$E_z = -B_x\left[M_{s1}t_1\cos(\phi_1) + M_{s2}t_2\cos(\phi 2) + M_{s3}t_3\cos(\phi_3)\right] - B_y\left[M_{s1}t_1\sin(\phi_1) + M_{s2}t_2\sin(\phi 2) + M_{s3}t_3\sin(\phi_3)\right]$$

Interlayer Exchange

$$E_{exc} = J_{RU}\cos(\phi_1 - \phi_2) + J_{AlO}\cos(\phi_2 - \phi_3)$$

Anisotropy

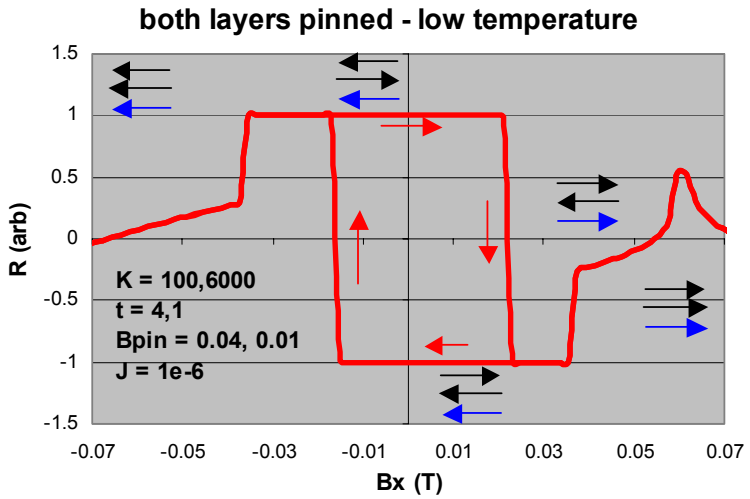
$$E_K = K_1t_1\sin^2(\phi_1) + K_2t_2\sin^2(\phi_2) + K_3t_3\sin^2(\phi_3)$$

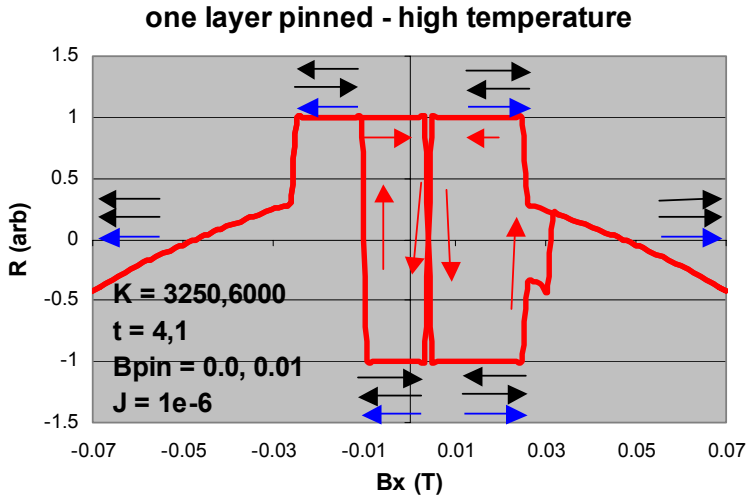
Demagnetization Fields

$$E_d = \frac{1}{2}\mu_0 t_1 M_{s1} H_{d1} + \frac{1}{2}\mu_0 t_2 M_{s2} H_{d2} + \frac{1}{2}\mu_0 t_3 M_{s3} H_{d3}$$

$$H_{di} = \begin{vmatrix} H_i^x \\ H_i^y \end{vmatrix} = \sum_{j=1}^{3} \begin{vmatrix} N_{xx}(i,j) & N_{xy}(i,j) \\ N_{yx}(i,j) & N_{yy}(i,j) \end{vmatrix} \begin{vmatrix} M_j^x \\ M_j^y \end{vmatrix}$$

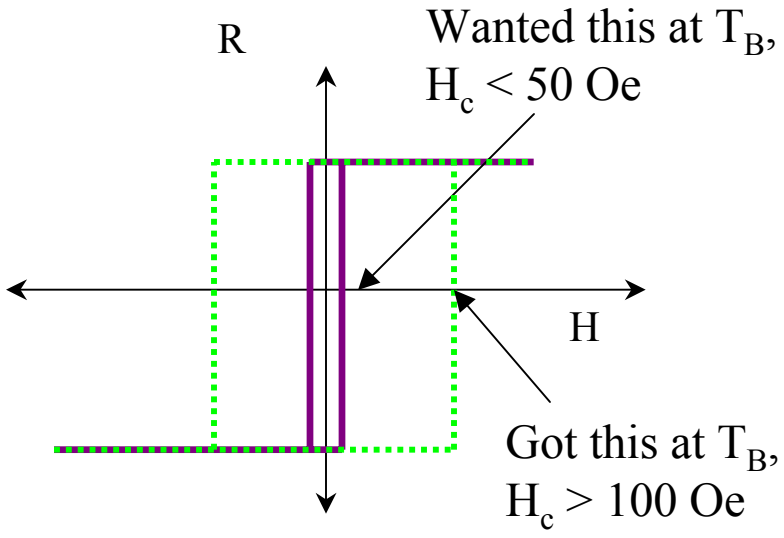
Simulated Response





Apparently

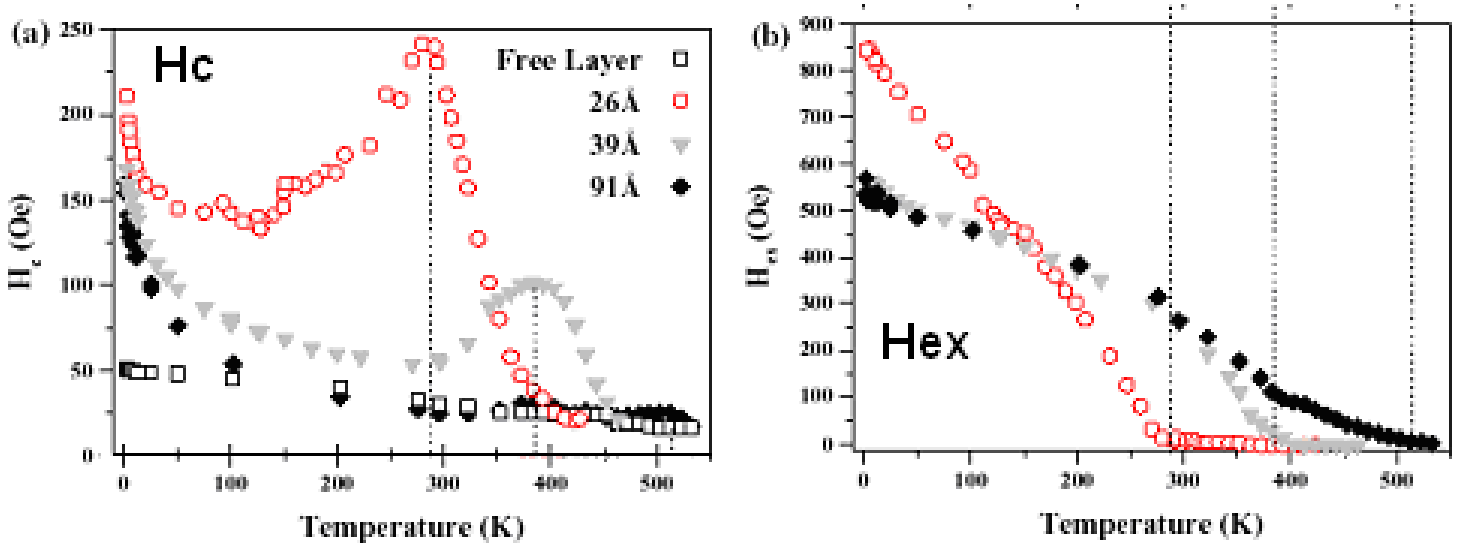
- H_c IrMn > (H_c + H_{ex}) PtMn
- And pinned layer SAF not well matched
- Coercivity of the storage layer is too high at T_B!



NVE CORPORATION

IrMn H_{ex} and H_c

Must increase IrMn layer to 60 nm

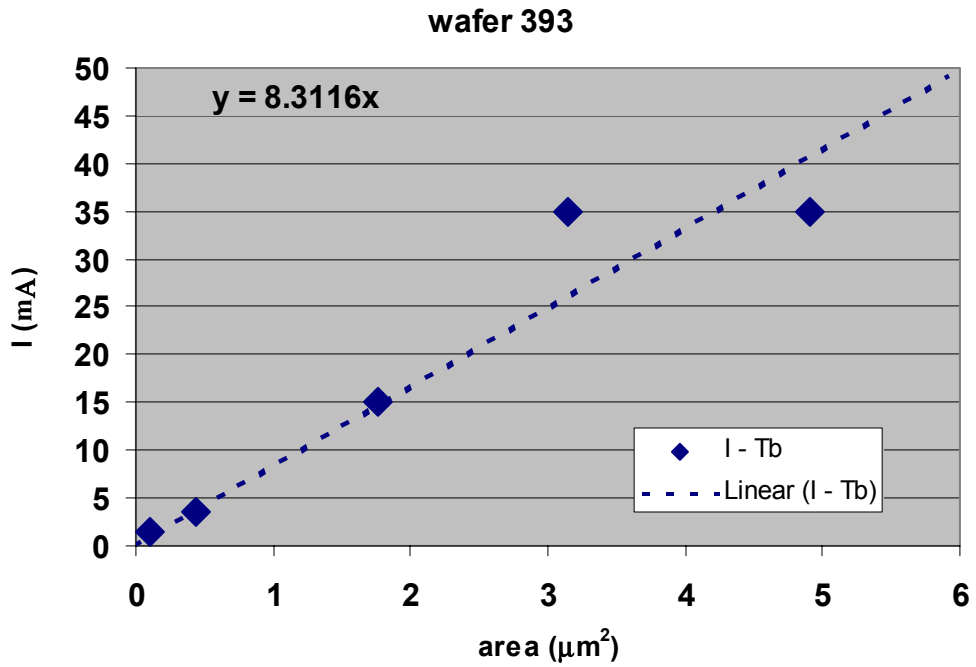


- Increasing thickness of IrMn decreases H_c and increases H_e.
- T_b would be increased 50 to 100 K.
- Increasing RA to 10 $\Omega\mu m^2$ would keep the write current at the present value and still permit safe writing

$$I(\Delta T) = A\sqrt{\frac{\Delta T 2K_v}{L_v\langle RA\rangle}}$$

Measured Programming Current

Current through barrier required to exceed T_b



8.3 mA/μm²

Using only a single barrier and no heater layers

100 nm bit → π*(0.1/2)*(0.1/2)*8.31 = 0.065 mA

Conclusions

- Demonstrated heating through the barrier, and potential for < 100 μA write currents at 100 nm dimensions
- IrMn thickness needs to be increased
- RA needs to be optimized, need roughly 50 $\Omega\mu m^2$
- Need to do a better job matching the SAF
- Lower thermal conductivity encapsulating material like BCB would further decrease write current
- If needed NOL heaters could be added to further decrease write current (at the expense of signal)