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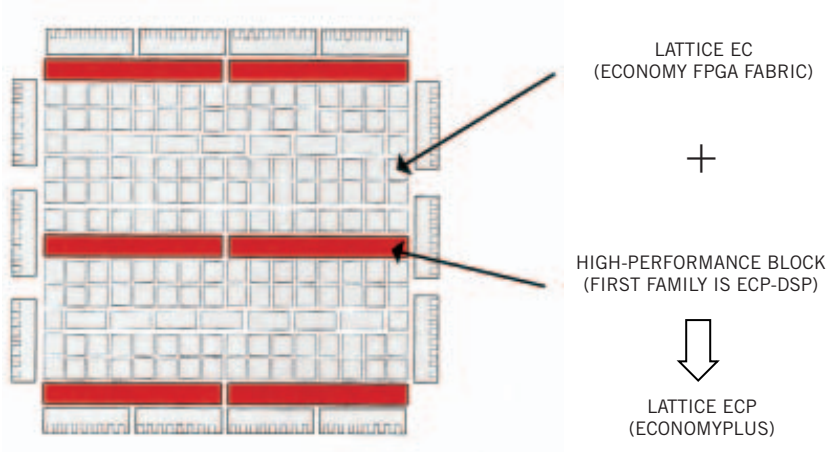
to make more efficient use of silicon area, and, unlike with Xilinx's Spartan-3, on which half of the LUTs (look-up tables) could find use as either logic or distributed RAM, only 25% of the LUTs on EC and ECP offer this flexibility. EC and ECP devices notably support industry-standard SPI-based configuration memories, along with traditional parallel and serial approaches.—by Brian Dipert

▶**Altera**, 1-408-544-7000, www.altera.com.

▶**Lattice Semiconductor**, 1-503-268-8000, www.latticesemi.com.



ECP devices, in the initial ECP-DSP implementation of the concept, interleave dedicated DSP blocks amid generic user-programmable logic and memory.

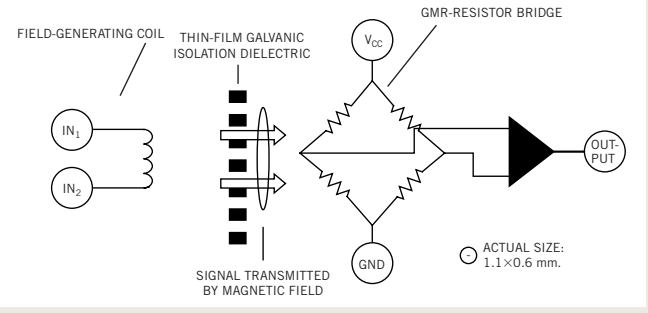
Monolithic digital coupler is small but intense

When you need to get a digital-logic signal from Point A to Point B without physical connection for either safety or performance reasons, you can use a galvanically isolated coupler based on capacitive, magnetic, or optical techniques. The IL6xx family of IsoLoop couplers from NVE Corp uses the GMR (giant-magnetorestrictive) principle at its core, with single- and dual-channel models. These couplers are the first available in die form, according to the vendor, so you can use them in hybrid and similar packaging techniques. The single-channel version measures 1.1×0.6 mm, and the two-channel version measures 3×3 mm.

The devices support a 40-Mbps data rate and feature 20-nsec typical propagation delay and 10-nsec delay skew. Partially due to the passive front end, which NVE based on a field-generating coil, power dissipation is only 1.4 mA at 3.3V and 2.5 mA at 5V, and input-threshold current is 10 mA. Isolation is 2500V rms for one minute; the devices operate at −40 to +85°C. They come in CMOS-compatible and open-drain output styles. The single- and dual-channel couplers sell for $1.35 and $1.98 (1000), respectively.

—by Bill Schweber

▶**NVE Corp**, 1-952-829-9217, www.nve.com.



Get your digital signal's point across without touching, using the GMR-based IsoLoop IL6xx monolithic couplers, which offer a 40-Mbps rate with 2500V rms isolation.

MEMS MAKE A NONVOLATILE-MEMORY MATCH

Although MEMS (microelectromechanical-systems) technology may seem an unlikely match for nonvolatile memory, Cavendish Kinetics says it's an excellent fit. The company offers IP (intellectual property) for building such memory on standard-CMOS processes with standard equipment and process steps. Cavendish positions this memory architecture as an alternative to embedded fuse, flash, and EEPROM structures. The MEMS memory works by flexing a microbeam that snaps in place to change bit states with applied voltage and stays when you remove that voltage.

Among advantages of this approach, says Cavendish, are 25-pJ programming energy—one-thousandth that of other memories—using the native 1.5V programming voltage and thus no dc/dc converter or charge pump. The technology also provides resistance to soft errors, 200°C operation, and extreme shock ruggedness due to low physical mass.

The company's initial IP is an e-fuse, which it will follow with an OTP (one-time-programmable) memory and then a multiple-time-programmable memory. In addition, Caven-dish says, this technology scales up in memory capacity and down to 25-nm fab processing and has a cost that is comparable with nonvolatile approaches.

–by Bill Schweber

▶**Cavendish Kinetics**, www.cavendish-kinetics.com.

▶**More than 430,000 people make all or most of their living selling on eBay.–*The Wall Street Journal*, June 17, 2004**