Current Perpendicular-to-plane GMR for Magnetoelectronic RAM

K. Bussmann, G.A. Prinz, S.-F. Cheng Naval Research Laboratory, 4555 Overlook Ave SW, Washington, DC 20375 USA J.-G. Zhu, Y. Zheng Carnegie-Mellon University, Pittsburgh, PA 15213 USA

J. M. Daughton, R. Beech, D. Wang

Nonvolatile Electronics Inc., 11409 Valley View Rd. Eden Prairie, MN 55344 USA R. Womack

High Density Circuits, 7820-2 Pan Am'n East Fwy NE, Albuquerque, NM 87109 USA

Introduction

Different avenues are being explored to realize non-volatile high density magnetoelectronic memory. Our work has focused on the applicability of the current perpendicular-to-plane configuration of magnetic multilayers showing giant magnetoresistance (CPP-GMR). Successful realization relies on overcoming several technological hurdles that include understanding the complicated transport characteristics and micromagnetics of the multilayer system, device fabrication, process integration to Si electronics, and the memory operating mode and architecture. In this work we present our results to date in our evolving approach to constructing a functional memory.

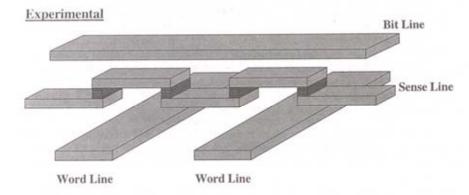


Fig 1. Basic sense line memory architecture.

Dr. Konrad Bussmann

Naval Research Laboratory 4555 Overlook Ave SW, Code 6345 Washington, DC 20375 USA

Tel: 202-767-4694 FAX: 202-767-1697

Email: bussmann@anvil.nrl.navy.mil

Figure 1 identifies one of the basic architectures we have used in exploring CPP-GMR MRAM. This layout is developed as a simple sense line array consisting of word and bit lines surrounding a magnetically active sense line. Magnetic information is stored in two magnetic multilayer stacks per bit that are selected by appropriate current drive through the bit and word lines. As shown in a plan view in Fig 2, the geometry utilizes one transistor per every other bit to perform a

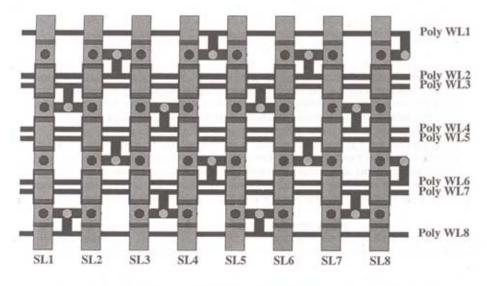


Fig 2. CPP-GMR MRAM layout.

pseudo-Kelvin measurement of the device resistance by passing the voltage excited by a sense line current through a bit to neighboring sense lines. The sense lines are connected to electronics operating at the borders of the magnetic array that are designed to differentially amplify the device signal and level-shift to standard I/O values. The all-metal construction of the magnetics allows simple processing steps in realizing the arrays. We have optimized a process for this architecture that utilizes various steps of chemical-mechanical polishing and ion beam milling that produces negligible contact resistance between the device and overlay metal lines. Magnetic mesas, typically multilayers of (NiFeCo/Cu/CoFe/Cu)_N resting on a copper underlayer, have been made with lateral dimensions down to 0.2 x 0.6 um.