Spin Dependent Tunneling Devices Fabricated Using Photolithography

Russell S. Beech, John Anderson, Jim Daughton, Brenda A. Everitt, and Dexin Wang
Nonvolatile Electronics, Inc., 11409 Valley View Road, Eden Prairie, MN 55344

***Abstract* — Spin dependent tunneling (SDT) devices have been fabricated using standard photolithographic techniques. The SDT film was RF diode sputtered NiFeCo(125Å)/Al_2O_3(20Å)/CoFe (125Å). Device resistances ranged from 1 KΩ to 12.9 KΩ for device areas of 1000 μm^2 (10 μm X 100 μm) to 84.5 μm^2 (6.5 μm X 13 μm), respectively. Peak GMR was over 4% at low bias with saturation fields around 10 Oe. Hard layer switching fields were about 50 Oe. Memory operation was demonstrated using integrated metallization for supplying read/write fields.**

I. Introduction

SDT materials are a GMR material which operate in a current perpendicular to the plane (CPP) mode. The basic film structure consists of two magnetic films that are separated by a thin insulating film. Changes in the magnetization orientations in the two magnetic films, relative to one another, result in a change in the tunneling current through the insulator - this gives the SDT magnetoresistance.

Because SDT devices utilize a tunneling current, they have very high resistance per unit area relative to other magnetoresistive materials. This makes SDT devices attractive for high density, low power applications. For example, using a 2μm linewidth, a resistor made from the multilayer GMR material that is used in commercial sensors would take up about 4,500 μm^2 for the same resistance (12.9 KΩ) as the 84.5 μm^2 SDT device reported here.

SDT devices also have the potential for very low saturation fields (~1 Oe). Because SDT devices use CPP, there is not a shunting problem for thick magnetic layers. Thus, the soft layer coercivity can potentially be made quite low by making it very thick - without causing a drop in GMR due to current shunting.

Previously published SDT results reported on relatively large (1 mm x 1 mm) devices that were defined using shadow mask sputtering [1], [2]. This shadow mask technique uses a mask, within the sputtering system, to sputter different patterns for each of the SDT material layers.

The devices reported on here were patterned and fabricated using standard semiconductor photolithographic and processing techniques. Thus, these devices can be made quite small and can be integrated with other devices and structures - such as transistor underlayers and metallization layers.

Manuscript received 1 March 1996.

This work was supported in part by: the National Science Foundation under Grant No. DMI-9461541, the Advanced Research Projects Agency under Agreement No. MDA972-95-3-0014, and the Naval Research Laboratory under Contract No. N00014-95-C-2255.

II. Processing

The SDT films were deposited using RF diode sputtering in a four target, load locked Perkin Elmer 2400 sputtering system. All three layers of the SDT film, plus a silicon nitride passivation layer, were deposited in situ. The insulating layer (20Å of Al_2O_3) was deposited using an Al_2O_3 target. All SDT layers were deposited with 100 watts of power in an Ar atmosphere, while the silicon nitride was sputtered at 350 watts. The magnetic layers, NiFeCo(125Å) and CoFe(125Å), were deposited in a 20 Oe field.

Following deposition, the BH loops of the films were checked for a double loop, characteristic of uncoupled, or weakly coupled, magnetic sandwiches. The quality and separation of these double loops is an indicator of the continuity of the insulating layer and the smoothness of the interfaces. If the insulating layer has substantial pinholing, the magnetic layers are strongly coupled and only a single loop is seen. Magnetostatic coupling and minor pinholing results in a sloped transition between loops and a decrease in the loop separation. The best films exhibited quite distinct double loops with separations of about 10 Oe.

Following deposition of the SDT film, four photolithographic steps and two depositions where required to finish SDT device fabrication. The first photolithographic step is used to define the bottom electrode of the SDT device (at this point, the patterned areas contain the entire SDT film). A second photolithographic step is used to define the active area of the device - the top magnetic layer is removed except in the active area. This second photolithographic step is followed by a second silicon nitride deposition. Once the nitride is deposited, a third photolithographic step is used to open up contacts to the top and bottom layers of the device. A subsequent metal deposition and photolithographic is used to fabricate bonding/test pads and corresponding metal interconnects between the pads and the SDT device. An optional fifth photolithographic step, nitride deposition, and metal deposition were used to deposit and pattern a bias strap across the top of the SDT devices. Fig. 1 shows both a top view and a cross section of the basic SDT device (without the bias strap).

III. Testing and Results

The SDT devices were tested using a constant voltage source and a 1 KΩ series resistance. The voltage source was adjusted to give a desired bias across the SDT device and then the voltage across the series resistor was recorded as a function of applied field. Using the fixed value of the series resistance and the total supply voltage, the data were transformed to yield the R-H curve of the SDT device.

Initial testing was done at the wafer level using a modified probe station fitted with Helmholtz coils Testing was done

at room temperature, with some low temperature testing done on packaged devices. An 8 pin DIP package style was used.

A. Basic Results

The three devices from which the following data were taken have active area dimensions of: 6.5 μm X 13 μm, 10 μm X 20 μm, and 10 μm X 100 μm. A representative R-H plot for one of these devices is given in Fig. 2. This plot shows the soft layer switching field (saturation field) to be roughly 10 Oe and the hard layer switching field to be about 50 Oe.

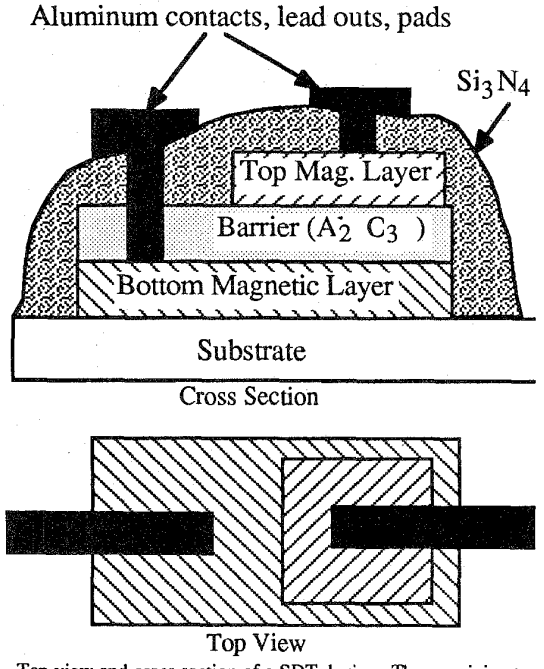

Fig. 1. Top view and cross section of a SDT device. The remaining top magnetic layer defines the active area of the device.

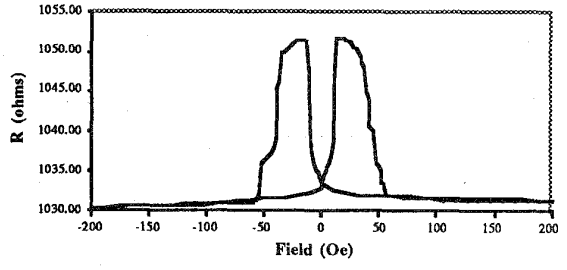

Fig. 2. R-H plot for a 10μmX100μm SDT device.

While wafer yield was low (25%), yield and uniformity across a wafer with working devices were very good. Not every device on a good wafer was tested, but for those that were tested (several hundred) the yield was 100%.

In addition to the R-H curve, the I-V curve of these devices was also plotted. The nonlinear characteristic shown in Fig. 3 is an indication that the primary current component is due to tunneling.

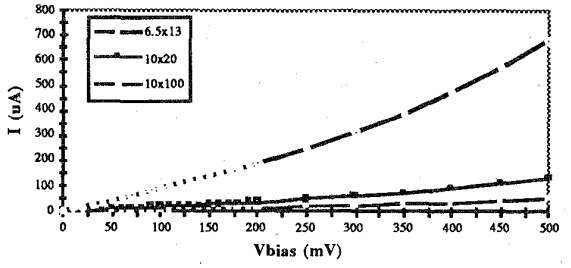

Fig. 3. Representative I-V curves for the three different SDT device types.

Another phenomena that has been observed in previous SDT work is a strong dependence of the GMR on the device bias voltage [1]. As shown in Fig. 4, the SDT devices reported here exhibit the same GMR-bias voltage relationship. It is hypothesized that the current resulting from the voltage bias has two components. One component is spin dependent and is responsible for the linear region of the I-V characteristics shown in Fig. 3. The other component is a non-spin dependent tunneling component accounting for the non-linear region of the I-V characteristics. If this is the case, then the decrease in GMR, shown in Fig. 4, would be due to the relative decrease in the spin dependent current component and the GMR would be directly proportional to ΔI(linear)/I(total). Further analysis has shown that the GMR decreases faster as a function of device bias than this ratio. Therefore, this simple model does not explain what is observed.

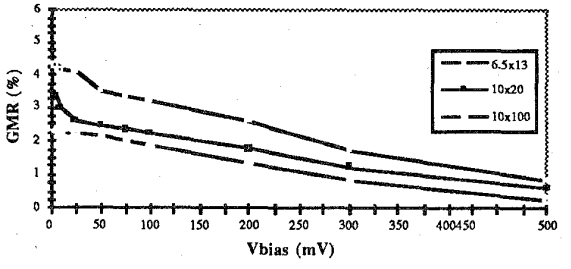

Fig. 4. GMR versus bias voltage for SDT devices. Based on this characteristic, these devices will be inherently low voltage, low power devices.

A few devices survived packaging and were used for low temperature testing, though their performance was somewhat degraded by the packaging process. These devices were tested at room temperature, cooled to 77 K, and then tested again. At liquid nitrogen temperature, the GMR was approximately double the room temperature value, the base resistance increased by 20%, and the saturation/switching fields increased substantially, with the hard layer switching field increasing from about 50 Oe to over 250 Oe. The increase in base resistance is much lower than would be expected if the resistance followed a T^2 law, as has been suggested [2]. Fig. 5 shows the R-H plot of a device at 77 K.

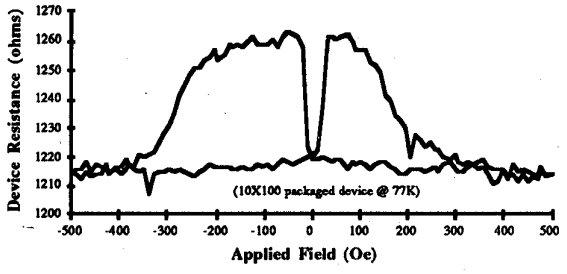

Fig. 5. R-H plot of a SDT device at 77 K. The hard layer saturation field has increased by a factor of 5 from the room temperature value. Base resistance has increased by 20%.

B. Applications

Two potential applications for SDT devices are magnetic field sensors and memory cells. For field sensing, the device should have high sensitivity to magnetic fields and an asymmetric response with respect to field polarity. Memory operation requires two distinct characteristics, to represent the logical "0" and "1" states, and the ability to "read" and "write" the state without external means - such as an applied field.

From Fig. 2, it is clear that the SDT device requires a bias field before it exhibits a linear response. The simplest way to generate this bias in an integrated device is with an integrated bias strap. Fig. 6 shows the SDT device characteristic when a current is passed through this bias strap. If the hard layer is properly "set", the result is an asymmetric response around zero field. This illustrates the proper characteristic for a magnetic field sensor.

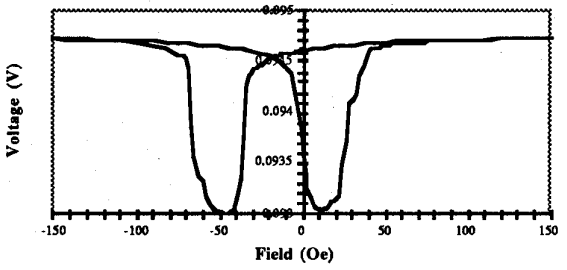

Fig. 6. SDT characteristic with a bias applied by an integrated bias strap. For the proper "set" of the hard layer, a bipolar response is obtained from bipolar fields.

Returning to Fig. 2, it is clear that two distinct characteristics exist between ±20 Oe - i.e. a positive or negative slope depending on the set of the hard layer. To be used as a memory cell, this characteristic must be interrogated and switched without external fields. Again, this can be accomplished with an integrated "word" strap. The two traces in Fig. 7 show the SDT device current as a function of word current. One of the traces was preceded by a +250 mA current pulse in the word line while the other trace was preceded by a -250 mA current pulse in the word line. As can be seen, these large current pulses wrote the SDT device to a "0" state or a "1" state.

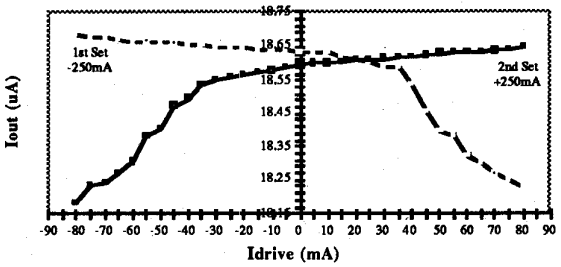

Fig. 7. "Read" traces of a SDT device following a write to a "0" state and to a "1" state.

These initial SDT devices are relatively large and the word strap is quite wide - covering the active area of the device. This results in undesirably large read and write current requirements. As the devices are made smaller and/or the word line is made narrower, the current levels will decrease. In practice, an array of these devices would use two lines for writing - requiring only half the current in each line (this half current could be routed through both lines during a write).

IV. Summary

The results reported here detail the successful fabrication of SDT devices using standard semiconductor processing and photolithographic techniques. In addition, these devices were integrated with metallization layers to add interconnects, bonding pads, and current straps for on-chip field generation. These current straps were used to demonstrate memory operation and biasing for bipolar field sensing. These devices are considerably smaller than those previously reported and were processed in a fashion that would allow full integration with IC electronics.

At low bias voltages, the GMR exceeds 4% and the saturation field is about 10 Oe. Hard layer switching fields are roughly 50 Oe. At 77 K, the GMR doubles, the hard layer saturation field increases by about 5X, and the base resistance increases by only 20%. For a working wafer, uniformity across the wafer is very good and yield is 100%.

References

[1] J. S. Moodera, Lisa R. Kinder, Terrilyn M. Wong, and R. Meservey, "Large magnetoresistance at room temperature in ferromagnetic thin film tunnel junctions," *Physical Review Letters*, **74**, pp. 3273-6, April 1995.

[2] T. Miyazaki and N. Tezuka, "Giant magnetic tunneling effect in Fe/Al_2O_3/Fe junction," *Journal of Magnetism and Magnetic Materials*, **139**, pp. L231-4, 1995.