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SCALING AND POWER OF THERMALLY WRITTEN MRAM

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Abstract— Current nonvolatile Magnetoresistive Random Access Memory (MRAM) designs that are being pursued by industry for commercial markets are not well suited to military and space missions. They consume a fair amount of power, making them unsuited for long battery-powered missions. They are not designed for radiation environments, requiring weight-restrictive shielding, and are susceptible to upsets caused by stray magnetic fields, which require additional magnetic shielding. This paper will focus on designs that are attempting to eliminate these restrictions for military and space applications. Most nonvolatile RAM technologies currently being developed use a transistor as a part of the memory cell. As photo lithography becomes smaller and smaller, this transistor becomes a significant part of the cell size. To keep this device small, on the order of the lithography, it is important to reduce the current through the cell. In addition, as elements are made smaller, the thermal excitation of the elements becomes progressively more important as a design consideration. To make the elements adequately stable, generally the anisotropy must be increased. Increased anisotropy means larger drive fields are required to switch the elements. Larger drive fields in turn require larger current densities in the conductors and this causes an increase in the accompanying heating. Thermal writing or thermally assisted writing exploit the heating that occurs and can be exploited to substantially reduce the drive currents which are required to write a memory element. A comparison is made between MRAM single free layer, toggle bits, Ru coupled free layer and several thermal write bits for scaling, writing, writing temperature and stability.

Index Terms— MRAM, Thermal Write, Tunnel Cell, RAD Hard

I. INTRODUCTION

The original MRAM used Anisotropic Magneto-Resistance (AMR) films, which were tested and shown to be radiation hard in memory applications. Current MRAM developments generally use a Spin Dependent Tunneling (SDT, a.k.a. Magnetic Tunnel Junction, or MTJ) magnetoresistive technology.[2][3] The SDT based MRAM has been found to exhibit the same radiation hardness in the storage-readout element as the AMR based MRAM. In radiation hard applications, a high speed, radiation hard, nonvolatile SDT MRAM can be used as a distributed memory to provide nonvolatile storage of coefficients and register data, or it can be used as main storage. SDT devices have been radiation tested to over 1 Mrad with no adverse effects. The current SDT memory being developed combines the inherently radiation hard SDT memory element along with circuitry on Silicon on Insulator (SOI) technology to obtain a robust RAD Hard component.

As elements are made smaller, the thermal excitation of the elements becomes progressively more important as a design consideration. In order to make the elements adequately stable, generally the anisotropy must be increased. Increased anisotropy means that larger drive fields are required to switch the elements. Larger drive fields in turn require larger current densities in the conductors and this causes an increase in the accompanying heating. Thermal writing or thermally assisted writing exploits the heating that occurs and can be exploited to substantially reduce the drive currents which are required to write a memory element.

An analysis was done which shows the drive current reductions that can be obtained by use of Curie point or Neel point writing for several cell structures [7]. The analysis shows that thermal write techniques can be extended to considerably smaller element sizes than can be achieved with magnetic writing. The comparison was made for seven different types of tunnel cells. The analysis is made for cells with minimum feature sizes of 0.09 microns and 0.06 microns because these are the anticipated steps in the lithography road map. Currently, most MRAM efforts are focused on Motorola’s toggle mode or the single free layer mode. A number of other proposed modes are included in the comparison.

Approximations are used for the fields generated by clad conductors, the demagnetizing fields from uniformly thick elements, and the effects of shape anisotropy which will result in approximate computed solutions**.** Uncertainty in insulation coverage also is a factor.

The analysis shows that for Motorola’s “toggle mode” of writing elements and single free layer elements, and all magnetically selected elements the absolute drive currents increase as cell size is reduced. Thermally assisted, 0.09 micron diameter elements require comparable currents for heating in comparison to the conventional, magnetically

written 0.09 x 0.18 micron elements. However as element size is further reduced the thermal write currents continue to diminish.

As noted above, elements with a minimum feature size of 0.09 and 0.06 microns were used as a comparison basis. It is also assumed that the magnetic material has a saturated moment (Ms) of 800 or 1000 emu in the operating temperature range. The shape, shape anisotropy, and material anisotropy are selected to meet design needs within the limits of practicality. For purposes of comparison, it is assumed that the memory design has a cycle time of 50 nanoseconds, read operations occur only half as often as write operations, and the memory contains 16 Megabits with a byte wide write.

In the approximate analyses which are made, the principal mode of thermal excitation (in which the magnetic sample is considered a single, uniform domain) will be used. A more precise analysis would consider all thermal modes. In general, the cells will be designed so that the thermally induced error rate at the maximum operating temperature for the memory chip is 1/10 of the failure rate per hour for the high quality semiconductor devices. For a very high quality memory chip, the failure rate is 10^{-9} per hour.

II. HARDENING MRAM COMPONENTS

Electronics in SDT devices have been tested with radiation levels to over 1 Mrad with Co^{60}, thus demonstrating their robustness in radiation environments. Since MRAM cells have been shown to be inherently radiation resistant, focus can be placed on the design and fabrication of the supporting electronics. MRAM fabrication at NVE Corporation is currently using the Peregrine Semiconductor Corporation's rad-hard process. Their process utilizes a proprietary Ultra Thin Silicon (UTSI) process for fabricating rad-hard integrated circuits using silicon-on-sapphire (SOS) wafers. They are able to process 0.45 micron lithography, which will mesh well with the lithography that NVE is currently using. Peregrine discussed their Rad-Hard capabilities and presented a road map at GOMAC 2001[1].

III. RAD HARD MRAM WITH COMMERCIAL FABS

Another approach is to use the Silicon on Insulator (SOI) process of a commercial fab along with the Radiation Hardness by Design (RHBD) approach to utilize the potential of commercial CMOS foundries to supply radiation hardened MRAM for space missions. In the RHBD approach, design techniques are used to mitigate the effects of total-dose, dose-rate, and single-event effects in integrated circuits. These designs can then be manufactured at commercial foundries to produce circuits that meet the requirements of space applications.

IV. RAD HARD UNIQUE SSDT CELL

A low power Magnetoresistive Random Access Memory (MRAM) that uses a novel Sandwich-Spin Dependent Tunneling (SSDT) memory bit is currently being constructed for RAD hard buffer and small main memories applications. The SDT memory cell has a sandwich film on one side of the tunnel junction and contains two select transistors - one that is used during readout and one that is used during writing. Figure 1 illustrates this cell structure, showing schematically both the SDT structure and the select transistors. To write the cell, the write select transistor is turned on, and a write current flows through the sandwich portion of the cell. This write current flows in the plane of the SDT film. For a read operation, only the read select transistor is turned on, and a small tunneling current is passed through the cell in order to generate a readout voltage. For a given read current, the readout voltage will depend upon the alignment between the magnetizations of the magnetic films that are adjacent to the top and bottom surfaces of the tunneling barrier.

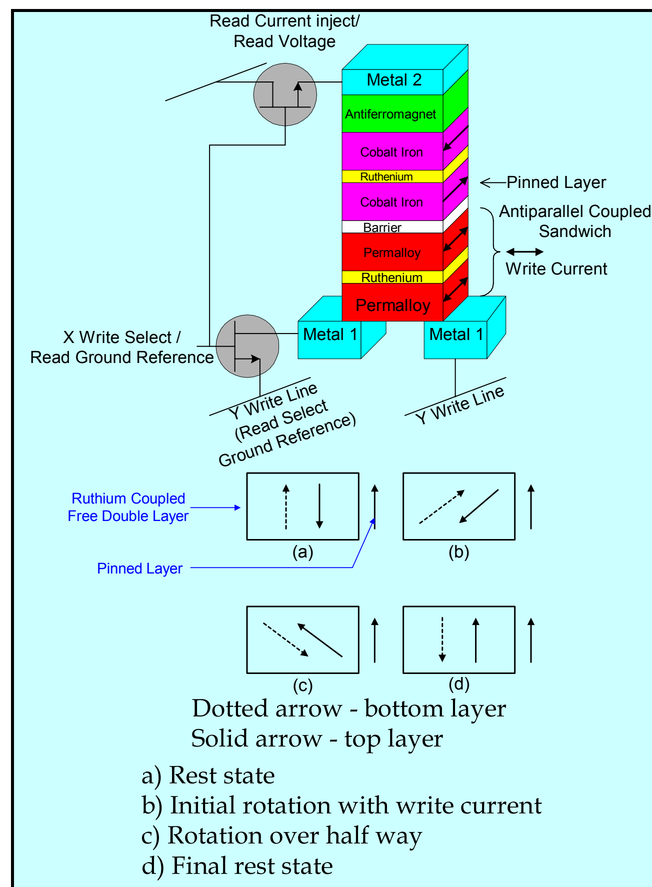

Figure 1. Schematic illustration of SSDT memory cell.

For the cell shown in Figure 1, the write current only flows through the selected cell. Since no write current flows through adjacent, non-selected cells, the half-select condition that exists in other MRAM is eliminated. Without

a half-select condition, the switching uniformity requirement is eased considerably. As long as the write current is set high enough to write the cell that has the highest write threshold, all cells in the memory can be written without disturbing a non-selected cell. Compared to the switching uniformity that is required for a 2D selection scheme, this single current selection scheme greatly improves the manufacturability of the memory. It is the combination of the sandwich storage element and the write select transistor that allows the single current selection scheme to work. In other MRAM cells, the write current flows through a separate current conductor - not through the storage element. The need for the separate conductor, combined with the sensitivity of other MRAM designs to disturb fields, makes it impractical to use the single current selection scheme with the other types of MRAM.

The second key feature of the SSDT latch bit is a significantly lower write current than other MRAM cells. This lower write current is due to the closed flux switching behavior of the anti-ferromagnetically coupled Ruthenium sandwich film that forms the storage element in the SDT buffer cell. Because switching involves a pair of magnetic films that are always aligned antiparallel to one another, the high demagnetization fields that are encountered during switching of a single layer film are avoided. Thus, smaller switching fields, and therefore smaller switching currents, are needed. This operation is illustrated in Figure 1.

The SSDT cell will be used in a Two Junction per Cell (2JC) architecture that uses a relatively simple latch cell circuit with one SSDT junction in each of the two halves of the latch cell. This architecture is shown schematically in Figure 2. The two SSDT devices are written to opposite states - one high resistance and one low resistance. To read the memory, the latch is momentarily shorted, so that both outputs are at the same potential, and then released. When the short is removed, the different resistance that is presented to the two halves of the latch, by the oppositely written SSDT junctions, causes the latch output to rapidly drive to a known logic level based on which SSDT junction is in a higher resistance state. This architecture is very fast and robust since the two cells provide high signal and act as local "references" for each other - there is no need to match closely to a reference cell that may be located a relatively large distance away.

The 2JC-memory architecture operates as a latch similar to that of SRAM. However, in radiation environments, it can be seen that the MRAM is more immune to upsets. If one of the transistors in the SRAM latch is upset, the data will be lost. The 2JC latch however contains the data in the SSDT cells, not the associated transistor. If one of those transistors is upset, it will have no effect on the data. The bit has a fully balanced circuit which is another key feature for radiation upset resistance.

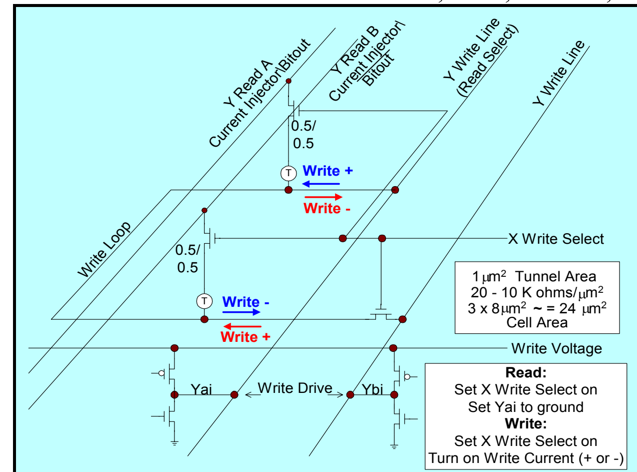

Figure 2. Schematic diagram of the 2JC memory architecture.

V. POWER AND DENSITY COMPARISON

In the following analyses for elements with magnetic selection, the following general assumptions were made about cladding and margins. For cells with a minimum feature size of 0.09 microns, the cladding is 200 Angstroms thick, the copper conductor extends 200 Angstroms beyond the element, a via has minimum feature size, and metal to metal spacing is 0.1 microns. For cells with a minimum feature size of 0.06 microns, the cladding is assumed to be 150 Angstroms thick and the copper conductors extend 150 Angstroms beyond the elements, a via has minimum feature size, and metal to metal spacing is 0.07 microns. For thermally assisted writing in which only one field conductor is needed, the cladding was allowed to extend below the copper conductor because shielding of the field is not a problem.

As a compromise between voltage headroom, trans-conductance, and transistor area, a 3.3 volt drive technology and a minimum transistor feature size of 0.1 microns was assumed. It was also assumed that the trans-conductance in saturation was 1 mA per micron of gate width. Although not necessarily optimum, the same assumptions were applied to all cell structures.

VI. TABLES OF CALCULATED RESULTS

SELECTED PARAMETERS

16 Megabit Die
3.3 Volt System
Gate length 0.1 microns, 1 mA/micron of gate width
Allowable Error Rate = 10^{-10}/ hour
Minimum Dimension = 0.09 or 0.06 microns
Area of Drive Transistors Included
Area of Read Selection Not Considered
50 nanosecond cycle time
Write fraction 33% or less
Material Ms = 800 emu or 1000 emu

Material Hk = 5 Oe or 15 Oe

TYPES OF TUNNEL CELLS CONSIDERED

A. Single Free Layer
B. Motorola Toggle Mode
C. Ru Coupled Free Layer & Multiple
D. Thermally Written Through Tunnel Cell (Neel Point
E. Thermally Written Through Tunnel Cell (Curie Point)
F. Multi-Pair, Round, Ru Coupled Free Layer

CRITICAL WELL DEPTHS & OPERATION

A. 59.3 KT, 350 K, ½ Select
B. 67.9 KT, 350 K, Rest State, 70% During Write
C. 59.3 KT, 350 K, ½ Select
D. 45 KT, 473 K, Write
E. 45 KT, 473 K, Write
F. 45 KT, 473 K, Write

SINGLE FREE LAYER

Item	0.09 micron minimum dim.	0.06 micron minimum dim.
Transverse Field Current	3.9 mA	5.6 mA
Write Field Current	4.8 mA	6.1 mA
Cell Effective Area in Array	0.155 microns squared	0.080 microns squared
Hw, Ht	193, 193 Oe	354, 354 Oe
Concerns	Vortex Formation	Vortex Formation

MOTOROLA TOGGLE MODE

Anisotropy Type	Tapered Ru; High Hk	Tapered Ru; High Hk
Item	0.09 micron Minimum Dim.	0.06 micron Minimum Dim.
Write Current I1	3.6 mA 4.6 mA	4.9 mA 7.2 mA
Write Current I2	4.0 mA 5.4 mA	5.7 mA 8.5 mA
Cell Effective Area in Array	0.158 microns squared	0.087 microns squared
H1, H2	193, 193 Oe 305, 305 Oe	355, 355 Oe 561, 561 Oe
Concerns	Alignment Material	Alignment Material

Ru COUPLED FREE LAYER

Item	0.09 micron minimum dim.	0.06 micron Minimum Dim.
Transverse Field Current	3.2 mA	4.5 mA
Write Field Current	4.0 mA	4.9 mA
Cell Effective Area in Array	0.154 microns squared	0.080 microns squared
Hw, Ht	155, 155 Oe	279, 279 Oe
Concerns	Threshold Uniformity	Threshold Uniformity

THERMAL WRITE THROUGH TUNNEL CELL (Neel)

Item	0.09 micron minimum dim.	0.06 micron minimum dim.
Tunnel Heating Current	0.1 mA	0.045 mA
Write Conductor Current	2.2 mA	2.7 mA
Cell Effective Area in Array	0.052 microns squared	0.025 microns squared
Write field	165 Oe	302 Oe
Concerns	Long Term Stability	Long Term Stability

THERMAL WRITE THROUGH TUNNEL CELL (Curie)

Item	0.09 micron minimum dim.	0.06 micron minimum dim.
Tunnel Heating Current	0.1 mA	0.045 mA
Write Conductor Current	3.4 mA	4.2 mA
Cell Effective Area in Array	0.08 microns squared	0.04 microns squared
Write field	160 Oe	294 Oe
Concerns	Vortex Formation	Vortex Formation

MULTI-PAIR, ROUND, Ru COUPLED FREE LAYER

Item	0.09 micron minimum dim.	0.06 micron minimum dim.
Transverse field Current	2.1 mA	2.0 mA
Write Field Current	2.0 mA	1.8 mA
Cell Effective Area in Array	0.093 microns squared	0.082 microns squared
Hw, Ht	90, 90 Oe	104, 104 Oe
Extreme Concerns	10.7 Angstrom Tolerance	3.4 Angstrom Tolerance

VII. ANALYSIS DETAILS

1. Single Free Layer Elements

For single free layer elements employing a Stoner-Wohlfarth threshold, half selected elements have a much reduced energy well depth, and therefore are the elements that may be thermally excited into an error state. If the maximum operating temperature is 77 degrees C, the thermal relaxation time is 10^{-9} seconds, and the chip size is 16 megabits with 511 + 1023 elements half selected, then the approximate required well depth for the elements in the rest state can be computed as indicated below.

$.5 * 10^{+9} * 1534 * 3.6 * 10^{+3} * e^{-(Eb/KT)} = 10^{-10}$

$Eb = 59.3\ KT = 2.87 * 10^{-12}$ ergs

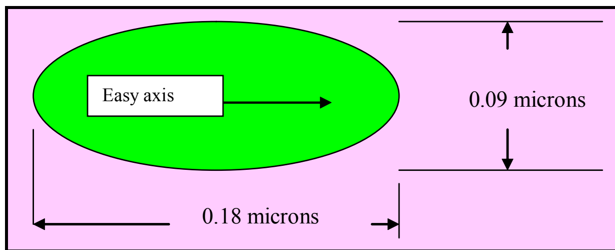

Figure 3. Free Layer Layout

Figure 3 above shows a 0.09 x 0.18 micron squared cell with a free layer thickness of 59 Angstroms which just meets this minimum energy requirement. The calculated shape anisotropy is 381 Oe and a near optimum drive point for the word and digit fields is ½ Hk.

Assuming 5 Oe of material anisotropy, then the required drive fields are 193 Oe. To meet these field requirements, square copper conductors clad with 200 Angstroms of permalloy on three sides are assumed. Copper conductors are necessary in order to span a large number of elements at low voltages. Figure 4 shows an on-top word line cross section.

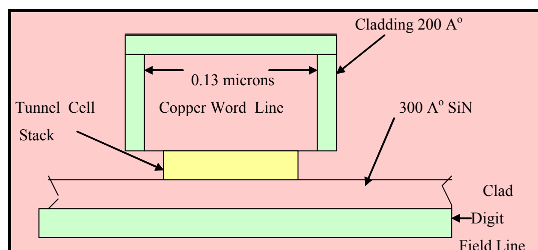

Figure 4. Clad Line Cross Section

The best density is obtained if the clad digit line is on the bottom and the clad line providing the transverse field is on top. To provide the required digit field from the clad, 0.22 squared conductor, a current of 4.8 mA is needed and the voltage drop per micron of length is 2.5 mV at room temperature. The transverse field line has a 0.13 micron square copper core and requires 3.9 mA. The voltage drop per micron of length is about 4.2 mV. For a 3.3 volt support technology, a basic 1024 x (512 or 1024) array is appropriate.

The spin dependent tunnel memory cells require selection and isolation transistors or diodes and they may very well be the limiting factor with regard to density. For simplicity, it will be assumed that they are not the density limiting factor. However, for the toggle mode or single free layer mode, room must be allowed for a via connection to the diodes or transistors in the silicon underneath. Figure 5 shows an approximate array layout with a minimum metal-to-metal distance of 0.1 micron spacing.

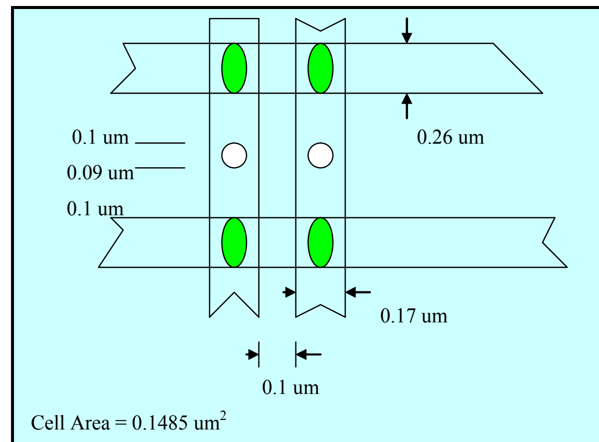

Figure 5. Cell Layout

To estimate the area taken by the drive selection transistors, it was assumed that the technology would provide at least 1 mA per micron of gate width and the transistors were of a general format. The gate length was assumed to be 0.1 microns with 0.1x0.1 micron squared vias.

The drive selection transistor requires only a little more than 6.2% of the area taken by a 1024 x 512 bit array so that the cell area plus the pro-rated drive selection transistor area is $0.155\ um^2$.

When the elements are scaled smaller by a factor of 0.6667 to a minimum feature of 0.06 microns, the thickness of the free layer must be increased by 1.225 to 72 Angstroms to maintain the required minimum energy well depth. The required drive fields increase to 354 Oe and the required currents are 5.6 mA and 6.1 mA. An appropriate array size is still 512 x 1024 even with the increased line resistance and current.

2. Toggle Mode Elements

In the Motorola toggle mode of writing coupled sandwich elements, two uni-polar fields are applied with one pulse following and overlapping the other [4][5][6]. The fields that the pulses generate are perpendicular to one another and are at an angle of 45 degrees with respect to the easy axis of the element as shown in Figure 6.

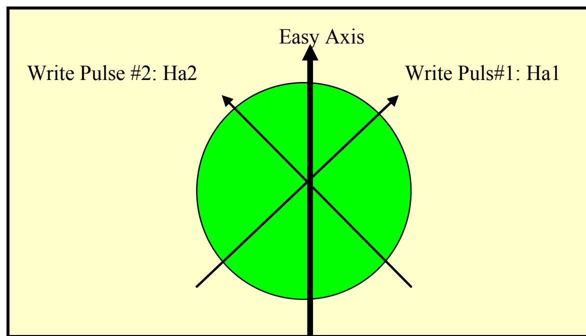

Figure 6. Toggle Mode Pulse Field Directions

The most critical mode for thermal failure for toggle mode elements occurs when the layer pairs are thermally agitated against the anisotropy field; all of the elements in the array are involved. In addition, during the switching process, an adequate well depth must be maintained (approximately 0.7 of static well depth). A near optimum set of parameters is to have the anti-parallel coupling field be 6.5 times the anisotropy field and to have the drive field 1.25 times the minimum value. In the design considered to meet this requirement, a circular sandwich 1.414 times the minimum feature with a non-uniform, minimum feature separation was assumed to provide additional anisotropy.

If the anisotropy field is Hk and the much larger anti-parallel coupling field is Hjd, the individual pulse field must have an amplitude of at least $Ha1 = (Hk*(Hjd+Hk)/2)^{.5}$ to initiate switching. If the maximum operating temperature is 77 degrees C, the thermal relaxation time is 10^{-9} seconds, and the chip size is 16 megabits, then the approximate required well depth for the elements in the rest state can be computed as indicated below.

$$.5 * 10^{+9} * 1.6 * 10^{+7} * 3.6 * 10^{+3} * e^{-(Eb/KT)} = 10^{-10}$$

$$Eb = 67.9 \text{ KT}$$

At 350 ^{o}K, $67.84*KT = 3.28 * 10^{-12}$ ergs

For a coupled sandwich to meet this requirement in an element 0.1273 microns in diameter, each layer must be 35 Angstroms thick if Ms = 1000 emu and the anisotropy field is 75 Oe. The anisotropy field assumed is composed of 15 Oe from the material and 60 Oe from the minimum dimension, shaped separation in the Ru. Using the ellipsoidal demagnetizing factor, the demagnetizing factor opposing scissoring of the couple magnetization (Hjd) is 558 Oe.

Hjd = pi/4 * 72 * 12,560/900 = 767 Oe

The required amplitude for one of the pulsed fields is then given by the following assuming a 25% margin.

Ha1 = 1.25*(75 *558/2)^.5 = 212 Oe.

To achieve the design field, the top conductor requires a current of 3.95 mA and the bottom conductor requires a current of 4.4 mA. Each line is capable of spanning five hundred or a thousand elements. For a layout similar to Figure 5, the array area per element is 0.1485 um^2. The drive selection transistors add less than 3.5% to the area for a 1024 x 1024 array so the effective area per element is 0.155 um^2.

If one reduces the dimensions of a toggle mode element by a scaling factor of 1/1.5 to 0.06 microns minimum feature, to meet the stability requirements, layer thickness must increase by 1.225 to 44 Angstroms, Hk to 138 Oe, and Hjd by 1.84 to 1027 Oe. The resultant drive fields are Hai = 355 Oe. The current in the top conductor needs to be increased to about 4.9 mA and for the bottom conductor increased to about 5.7 mA. Because of the increased current and resistance, the line can span only 512 to 1024 elements easily rather than both at 1024. Also the percentage of the area associated with the drive selection transistors increases from about 3% to 10%.

In the above analysis, the 75 Oe anisotropy was achieved with a non-uniform separation layer. If material can be found with a material anisotropy of 75 or 138 Oe and with a Ms of 1000 emu, then the elements can be made with a minimum feature diameter. For elements 0.09 microns in diameter, the layers must be 69 Angstroms thick, Hk = 75 Oe, Hjd = 1512 Oe, H1,2 = 305 Oe, and required drive currents are 4.6 and 5.4 mA. For elements 0.06 microns in diameter, the layers must be 85 Angstroms thick, Hk = 138 Oe, Hjd = 2904, H1,2 = 561 Oe, and required drive currents are 7.2 and 8.5 mA. A basic cell size saving of about 16% is achieved. Vortex formation may be a problem.

3. Ru Coupled Free Layer

With a single free layer with the dimensions considered, vortex formation is a serious concern. This problem can be alleviated by using a Ru coupled layer. Figure 7 illustrates a Ru coupled free layer made with ternary alloy with a Ms of 1000 emu and the material anisotropy increased to 15 Oe and with 85 Oe of shape anisotropy. With the 60 and 15

Angstrom thickness given, the well depth meets the minimum requirements.

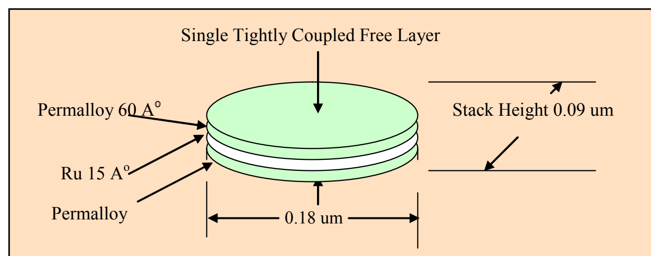

Figure 7. Ru Coupled Free Layer

The drive currents of 3.2 mA and 4.0 mA are slightly diminished from those for a single free layer because of the assumed increase in material anisotropy. When the elements are scaled to a minimum dimension of 0.06 microns, the thickness of the layers increases by a factor of 1.225 and drive fields increase by a factor of 1.84. The required drive currents are 4.5 and 4.9 mA When drive transistor area is included, the effective array areas are 0.155 and 0.08 microns squared for the cells with minimum features of 0.09 and 0.06 microns respectively.

3B. Multi-Pair, Round, Ru Coupled Free Layer

For purposes of comparison, a free layer made of multiple coupled layers is also examined; it is assumed that a material with a uniaxial anisotropy of 100 Oe is available with a Ms of 800 emu. It is also assumed that it is possible to etch almost perfectly round samples with the information maintained by the material anisotropy. To meet the well depth requirement for thermal stability of half selected elements with a width of 0.09 microns, 5 repetitions of a 70-20 Angstrom Ru coupled sandwich are required. The free layer disk would be 900 Angstroms in diameter and 500 Angstroms thick. Allowing a maximum variation in anisotropy of 5% and a maximum skew of 16 degrees, the element must be circular within 10.7 Angstroms. A circular bit distorted to an elliptical shape by 10.7 Angstroms could cause failure. For a free layer 600 Angstrom in diameter, 7 repetitions of an 80-30 Angstrom Ru coupled sandwich would be required with a total thickness of 882 Angstroms. In this case, only 3.4 Angstroms of elliptical distortion could cause failure. **Thus a nearly impossible fabrication precision is necessary to make reliable elements of this type.**

4. Thermally Written Cells with Tunnel Current (Neel)

Thermally writing cells with tunnel current is by far the most attractive way to write this type of cell for three primary reasons. This method of writing leads to the highest density, the smallest drive currents, and the largest margins. Both array area and drive currents are reduced by a factor of 2 or 3. This arrangement exploits the selection arrangement which is present for reading. However to get adequate heating, tunnel cells with the ability to carry 50 to 100 micro amps are required along with enhanced dissipation techniques such as double junctions, non-linear resistors, or dielectrically isolated CMOS.

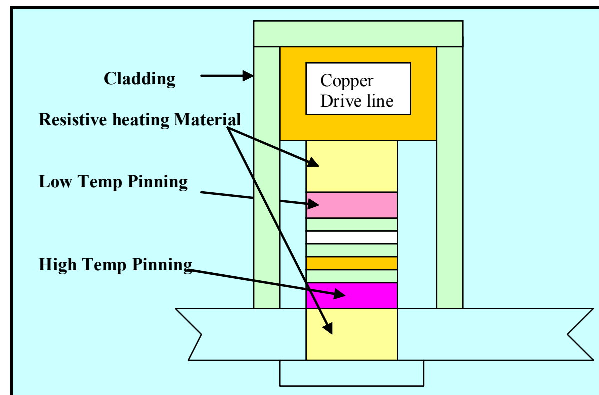

Figure 8. Thermally Written Pinning Cell Structure

Figure 8 shows that by use of sidewall insulation the cladding can be extended to provide larger fields for a given current and that the connections can be designed to provide additional heating. Note that only one drive conductor is required rather than two.

The well depth requirements are the same as for the coincident thermal heating, but with obvious space savings. Heating can be enhanced by several methods such as double junctions, resistive connections, or dielectrically isolated selection devices. Reasonable heating currents through the tunnel structures for the devices with minimum feature sizes of 0.09 and 0.06 microns are 0.1 and 0.045 mA. The associated top conductor currents which provide the setting fields are 2.2 and 2.7 mA respectively.

5. Thermal Written Cells With Tunnel Current (Curie)

For the case of cells where low Curie temperature is used, shape anisotropy is exploited to store the written information so a round element cannot be used. In the calculations which were performed, an element with a length to width ratio of 2 to 1 was assumed. Obviously, the cell area is increased. Figure 9 shows the structure.

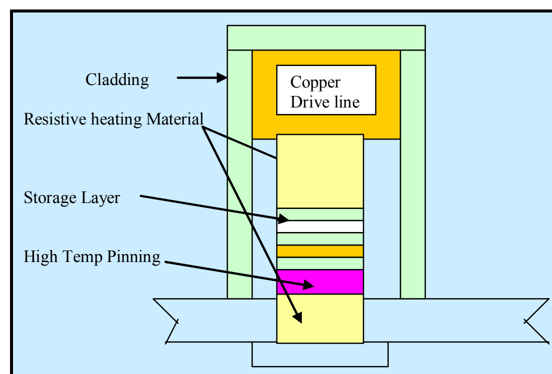

Figure 9. Thermally Written Cell with Tunnel Current (Curie)

As noted previously, the cell should "latch" when the magnetization reaches 1/3 of its room temperature value; as a consequence, the effective thickness of the information layer must be 29 or 35 Angstroms respectively for the cells with 0.09 and 0.06 micron minimum features. The design tunnel currents are 0.14 and 0.067 mA. The writing field current are 3.4 mA and 4.2 mA. If vortex formation is a problem, the information layer can be made from a Ru coupled sandwich.

VIII. CONCLUSION

A novel MRAM design that uses a sandwich-tunneling bit (SSDT) has unique write properties eliminating the high power and uniformity problems that have plagued previous MRAM designs. Design and layout of a 256 bit MRAM, using the SSDT bit, have been completed and test circuits with this bit are operational.

The write process of the SSDT bit, using a scissoring current that passes through the bit and produces closed flux switching in the antiferromagnetically coupled sandwich, significantly lowers the write current requirement of the memory. Typical SDT designs use two write currents of about 4 mA each, while the SSDT design uses a single current of about 0.8 mA - an order of magnitude improvement. The SSDT memory cell used in a latch bit configuration has been shown to be very stable in a radiation environment because of the MRAM resistance and the balanced scheme of the bit design. Since the disturb issues have been eliminated, it can be readily produced. However, it has size limitations for large size memories which will be solved in the future by using the thermal write configurations described in this paper.

The analysis shows that as tunnel memory cells are scaled to very small dimensions, thermally written cells have diminishing or near constant absolute current requirements while those for magnetically written cells have increasing current requirements with heating and current density limitation. The thermally written arrays require considerably less area for two reasons. The Neel type thermally written elements can be round rather than elliptical and a contact can be made directly below the cell so a provision for an extra via need not be made.

Thermally written cells with tunnel current is by far the most attractive way to write small tunnel cells for three primary reasons. This method of writing leads to the highest density, the smallest drive currents, and the largest margins. Cell area and drive currents are reduced by a factor as much as 2 to 5 in comparison to magnetically written cells and margins are large because only the selected element is heated. However, a great deal of work needs to be done with regard to achieving adequate heating with tunnel current.

IX. ACKNOWLEDGMENT

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