Address line-assisted switching of vertical magnetoresistive random access memory (VMRAM) cells

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Presentation Outline

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VMRAM Overview

- VMRAM = Vertical Magnetoresistive Random Access Memory
- Devised and developed by researchers at NRL and CMU
  - NRL: Dr. Gary Prinz\textsuperscript{1,2,3}, Dr. Konrad Bussmann\textsuperscript{2}
  - CMU: Dr. Jian-Gang Zhu\textsuperscript{1}
- VMRAM cells consist of toroid-shaped elements that have a stable closed-flux magnetic configuration
- Employs current perpendicular to the plane (CPP) to switch soft (read) and hard (write) magnetic layers of a GMR multilayer
- Address (word) lines generate radial torque fields that assist switching
- Teams from NVE Corp. and NRL have developed processes to fabricate 64-bit strings of 0.6μm O.D./0.2μm I.D. cells with address lines
- VMRAM is a high-density, non-volatile memory theoretically scaleable to 400Gbits/in\textsuperscript{2} at $\lambda = 10$nm\textsuperscript{1} and has the potential to compete with both semiconductor memories and mechanical hard disks.

\textsuperscript{3}G. Prinz, U.S. Patent No. 5477482
VMRAM Technology – Bits and Sense Lines

- 2000Å CMP’d Cu
- 40Å Ta phase breaking layer
- Multilayer stacks: \([\text{NiFeCo (20Å)/Cu (40Å)/NiFeCo (40Å)/Cu (40Å)}] \times 5\)
- 2000Å Cu connects cells such that current flows vertically
- Test arrays consist of 256 bits in 4x64-bit strings
VMRAM Technology – MR Response

- Response shape is similar to pseudo-spin valve
- Thicker (hard) layers act as storage mechanisms
- Thinner (soft) layers act as read mechanisms
- Simulated Response
  - Soft layers switch ~15 mA
  - Hard layers switch 40 – 55 mA
- Address line current effectively reduces switch thresholds
VMRAM Technology – Writing/Reading

Writing

Engage address current
Write from "1" to "0"

Reading

Soft layer minor loop

Engage address current
\[ v = i \Delta r \]
VMRAM Technology – Array w/ Address Lines

- Serpentine arrangement yields orthogonal upper/lower address lines
- Address current generates an outward radial word field for the current direction shown
- 4x64 arrays (4x8 section shown)
  - 4 sense lines run vertically
  - Address lines run horizontally
- 2-D selection
- Top and bottom address line segments connect through vias
- VMRAM cells reside at the junctions – 32 cells shown
Test and Analysis – General Test Procedure

- Run bipolar sense current sweep to determine switch thresholds (+/- $I_{th}$)
- Establish reference by saturating bits with $+I_{th}$ mA and sweeping the sense line with the same polarity current
- Saturate sense line with $< |-I_{th}|$ mA and $I_{addr}$ mA
- Sweep sense current from $+I_{small}$ mA to $+I_{th}$ mA
- Read voltage at each sense current step:
  - Sample voltage
  - Assert address current
  - Sample voltage
- Generate MR transfer curve
- Scale data by subtracting out reference curve
Test and Analysis – MR Response

- Observations:
  - GMR <1% vs. 10%-20%
  - Smooth transitions for hard and soft layers vs. abrupt switching

- Suspected cause: magnetic material redeposition
  - couples the stack layers
  - limits antiparallel alignment between hard/soft layers
  - and/or, significantly reduces the number of “active” layers
Test and Analysis – Read Layer

Soft Layer Switching (10 bits)

$I_w = 10mA$

Normalized PR

Sense Current (mA)

@ 4mA
@ 3mA
@ 2mA
Hard Layer Switching (10 bits)

$I_w = 11mA$

Normalized $\tau R$

Sense Current (mA)

@ 11mA
@ 12mA
@ 13mA
@ 14mA
@ 15mA
@ 16mA
Test and Analysis – Switching Asteroid

- Soft layer operating point
  - $I_{\text{sense}} = 6\text{mA}$
  - $I_{\text{addr}} = 5\text{mA}$

- Hard layer operating point
  - $I_{\text{sense}} = 12\text{mA}$
  - $I_{\text{addr}} = 10\text{mA}$

- Experimental data tends toward simulated $10\text{Å}/30\text{Å}$ combination

**VMRAM Switching Asteroid**

**Experimental vs. Simulated**

![Graph showing experimental vs. simulated data for VMRAM switching asteroid.](image)
VMRAM 2K IC Prototype Design

- Bonding pads
- Control logic
- 2 - 4x256 VMRAM arrays
- Decoder circuitry
- Sense amplifier
VMRAM vs. HDD (Projected)

- VMRAM Density at $\lambda = 0.01\mu m$ node
  - Best case: $16\lambda^2 = 403$ Gbits/in$^2$
  - Worst case: $18.77\lambda^2 = 358$ Gbits/in$^2$

- VMRAM compared to a 147GB HDD*
  - $\lambda = 0.09\mu m$ node
  - 9mm x 9mm PLCC package can hold 270 – 305Mb
  - HDD$^*$ FF $\Rightarrow$ 4” x 5.78” x 1.03”
  - Same sized VMRAM memory module yields 65 – 75GB
  - A VMRAM memory module built today could have $\sim$50% the capacity of today’s HDD
    - At $\lambda = 0.08\mu m$ (ITRS projection for 2005) capacity is $\sim$65%

- VMRAM has no mechanical wearout
- Smaller, rugged, more versatile form factor

*Maxtor Atlas$^0$ 15K II
Conclusion

- Four by sixty-four bit VMRAM test arrays were successfully fabricated using address lines designed for 2-D selection.
- Address-assisted switching of VMRAM cells was demonstrated
  - Soft layer switching: $I_{\text{sense}} = 6\, \text{mA}$, $I_{\text{addr.}} = 5\, \text{mA}$
  - Hard layer switching: $I_{\text{sense}} = 12\, \text{mA}$, $I_{\text{addr.}} = 10\, \text{mA}$
- Edge pinning in the GMR stack due to magnetic material redeposition led to low signal response and smooth transitions in unassisted MR response.
- GMR multilayer optimization is needed in order to maximize signal and ensure "singular" switching thresholds for stack magnetic layers.
- Integrated 2K VMRAM prototype design has been completed for a 0.35µm gate length semiconductor process.
- Hard and soft layer switching asteroids generated from experimental data compare well with micromagnetic simulations.

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