

# Spin dependent tunneling devices fabricated for magnetic random access memory applications using latching mode

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Spin dependent tunneling (SDT) devices were fabricated as building blocks for magnetic random access memory (MRAM) applications using latching electronics. The basic SDT structure was NiFeCo/Al<sub>2</sub>O<sub>3</sub>/CoFe/IrMn deposited using rf diode sputtering. The SDT structures and the word and torque coils were patterned using standard photolithography techniques. The junction magnetoresistance was 25.6%, the switching field was 12 Oe, the junction resistance-area product was 116 k $\Omega$   $\mu\text{m}^2$ , and the pinning field was 150 Oe. There were two legs of SDT resistors in a latch cell, with each leg consisting of at least one pair of junctions. The basic latching function of the devices was evaluated using external electronics. The two memory states per cell were demonstrated by passing a current of 22 mA with both polarities through the on-chip word coil. This translates to a field efficiency of about 1 Oe/mA for the word coil, which can be further improved by adding a magnetic keeper layer. The raw output voltage change was 21 mV for a SDT cell with four junctions and 4.5 k $\Omega$  resistance in each leg using a 50  $\mu\text{A}$  sense current. These results show great potential for SDT materials to be used in high speed and low power MRAM applications with latching mode.

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## I. INTRODUCTION

Spin dependent tunneling (SDT) junctions have high potential for the next generation magnetic field sensing devices primarily due to their high sensitivity and high resistance.<sup>1,2</sup> Possible application areas are low field/low power magnetic field/electric current sensing, galvanic isolators, magnetic switches, magnetic random access memory (MRAM) and other derivative applications.<sup>3,4</sup> For memory applications, the write selection can be done using both word and torque lines; the read selection can be done either using a transistor per cell with a reference, or using a latching mode as used in semiconductor static random access memory (SRAM).<sup>4</sup> The greatest advantages of this latter memory mode are the very high speed and very low power consumption in read operation, because it requires no word nor torque current to switch or even interrogate the magnetizations. Instead, the reading is steered by the two remanent states of the two legs of SDT resistors, e.g., high/low for ‘‘1’’ and low/high for ‘‘0.’’ SDT latch memory has potential for niche memory applications where unlimited read cycles and high speed are required and where low power consumption and nonvolatility are essential. This work uses external electronics to explore the possibility of using SDT resistors in this memory mode with on-chip current to write.

## II. EXPERIMENTS

The films were deposited using rf diode sputtering in a PE2400 system equipped with four 8 in. targets, a single wafer load lock, and a water-cooling wafer chuck. The alu-

minum oxide barriers were formed by plasma oxidizing a thin Al layer. The substrates were 4 in. Si(100) wafers coated with 2000 Å of Si<sub>3</sub>N<sub>4</sub> by low pressure chemical vapor deposition. The base pressure was lower than  $1.5 \times 10^{-7}$  Torr before deposition. A magnetic field of 20 Oe was applied during magnetic layer deposition to induce an easy magnetic axis. The entire deposition process was computer controlled. The patterning was done using standard semiconductor photolithography techniques<sup>5</sup> with dry etching steps. The process includes three layers of metallization. The basic magnetoresistance (MR) tests were done using an automated probe station with Helmholtz coils to provide the magnetic field. The latching function was tested using external electronics including two pulse current generators, two adjustable resistors for bridge balancing, a constant current source for sensing, an oscilloscope for displaying, and a probe station for making connections.

## III. RESULTS AND DISCUSSION

The magnetic field dependence of the MR for a typical SDT junction is shown in Fig. 1, with a major MR trace as inset. The junction MR is 25.6% from the major loop, the switching field is 12 Oe, the junction resistance-area product (RAP) is 116 k $\Omega$   $\mu\text{m}^2$ , and the pinning field is 150 Oe. Details on the SDT structures and thermal stability are described elsewhere.<sup>5,6</sup> These static properties will be compared with those seen when switching with on-chip write currents.

Figure 2 shows a schematic of a latch SDT memory bit including the SDT cell and the latching transistors. The operation of the latch SDT memory is similar to a semiconductor SRAM cell except with SDT resistors replacing some of

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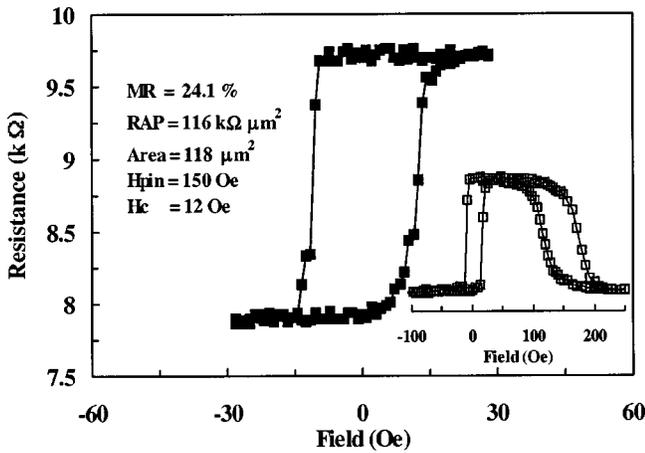


FIG. 1. MR traces of a pair of NiFeCo/Al<sub>2</sub>O<sub>3</sub>/CoFe/IrMn SDT junctions. The MR ratio is 25.6% from the major loop, as shown in the inset, with a bias voltage of ~100 mV for each junction. The resistance-area product (RAP) is 116 kΩ μm<sup>2</sup> and the pinning field (H<sub>pin</sub>) is about 150 Oe.

the transistors. When the circuit is powered up, the two terminals to the output buffer, Q and Q̄, will have either a “high/low” or “low/high” relationship, which can be assigned as a 1 and a 0. A test setup is built to test the latching function of the devices, as shown in Fig. 3.

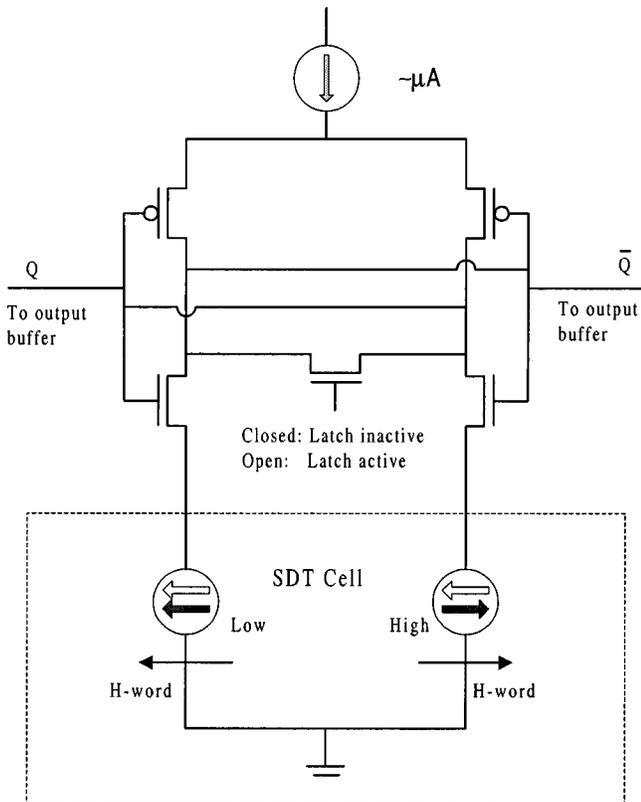


FIG. 2. Schematic of a SDT latch cell with two legs of SDT resistors and the latching transistors. Only the SDT part, along with the word and torque coils as marked within the dotted box, was fabricated on the wafer. The gray arrows in the SDT cell represent the free layer magnetization in the SDT structures; the open arrows above them represent the pinned direction. The resistance of a SDT junction is low when the free and pinned layer magnetizations are parallel.

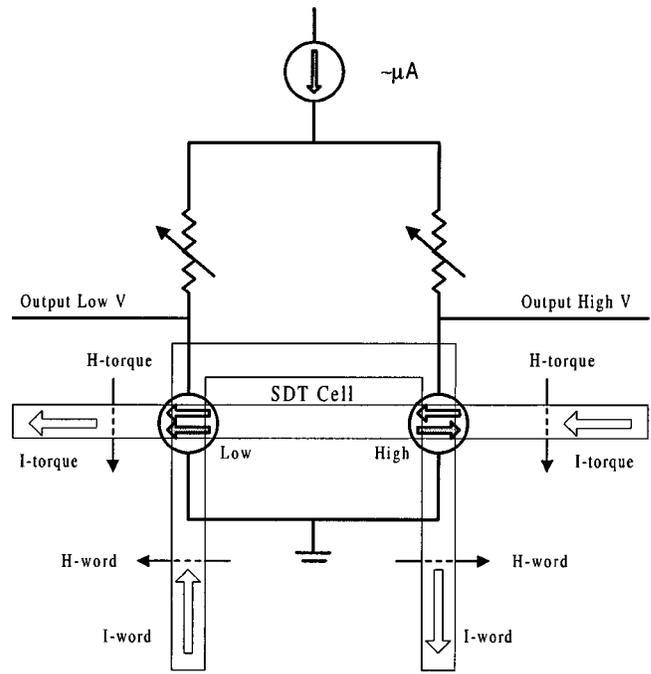


FIG. 3. Schematic of the test setup to evaluate the SDT latch cells using external electronics. The word field is supplied by passing a current through an on-chip word coil lying over both legs of SDT resistors but with opposite polarities. The torque field is applied by passing a current through a separate torque coil lying above the word coil.

Typical output voltage from the SDT resistors as driven by on-chip current is shown in Fig. 4. The general slope and the distinct steps in the loop are from the magnetostatic interactions among the free layers in the SDT devices. There is a distinct bee-waist shape in the loop, caused by the effective coupling between the free and the pinned layers. Because both legs of SDT resistors have the same pinning direction but the driving fields are in opposite directions, the width of the plateau in the loop is twice as much as the effective

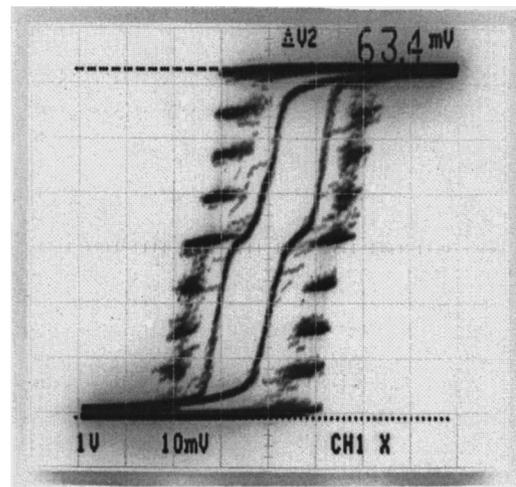


FIG. 4. Hysteresis loops of the sense voltage in response to a sweeping on-chip word current, with a sensing current of 50 μA. The inner loop is with an additional constant torque current of 10 mA. The vertical scale is 10 mV per division, and the horizontal scale is 10 mA per division. The inner loop is with an additional torque current of ~12 mA.

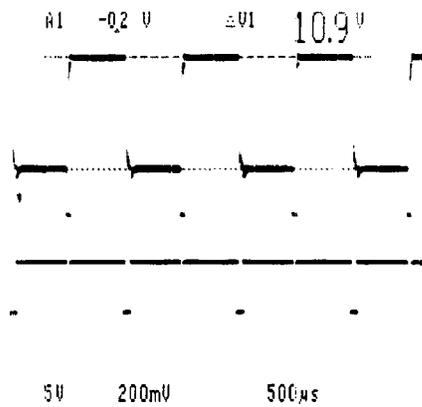


FIG. 5. Switching and latching characteristics for a typical SDT latch cell tested with external electronics as shown in Fig. 3. The bottom wave form is the on-chip word current with short pulses of  $\pm 22$  mA. The top wave form is the sense voltage signal from the two legs of SDT resistors using a  $50 \mu\text{A}$  sense current source.

coupling field. The switching current of  $\sim 12$  mA corresponds to a field of  $\sim 12$  Oe, translating to a field efficiency of roughly  $\sim 1$  Oe/mA, which could be further improved by using a magnetic keeper layer on top of the drive coils. It is noted that the latching functionality will not be affected by the drifting of the switching thresholds. As long as the two remanent states are achieved, the latch cell will function properly. Furthermore, when pursuing large memory arrays, it is likely that the number of junctions in each latch cell will be smaller, leading to a smaller slope and better stability of the remanent states. The effect of the torque current can also be seen from the inner loop in Fig. 4. The coercivity becomes smaller as the torque current of 12 mA is added.

Typical behavior of switching by word current and latching is shown in Fig. 5. The lower wave form is the coil current with short positive and negative pulses of 22 mA. The upper wave form is the output voltage from the SDT resistors showing a magnitude of 432 mV after being amplified and with a gain of 20 and using a constant sense current of  $50 \mu\text{A}$ . The raw sensing voltage swing is therefore about 21 mV. It is clear that after a short positive word current pulse the sense signal switches to high and stays at high, after the word current is turned off, until a negative word current pulse is applied. After the negative word current pulse is off, the sense signal stays at low until a positive word current pulse is applied. This clearly demonstrates the latching of the two remanent states due to the free layer switching.

Switching and latching behavior by a combination of word and torque currents for a typical SDT cell is shown in Fig. 6. There are three wave forms; the middle wave form is the word current with short positive and negative pulses of 12 mA. The bottom wave form is the torque current pulses of 12 mA with one polarity, and the top wave form is the amplified output voltage from the SDT latch cell showing a magnitude of 270 mV. It is clear that a torque current of 12 mA alone changes the sense signal only slightly but a combination of word and torque currents is enough to switch the

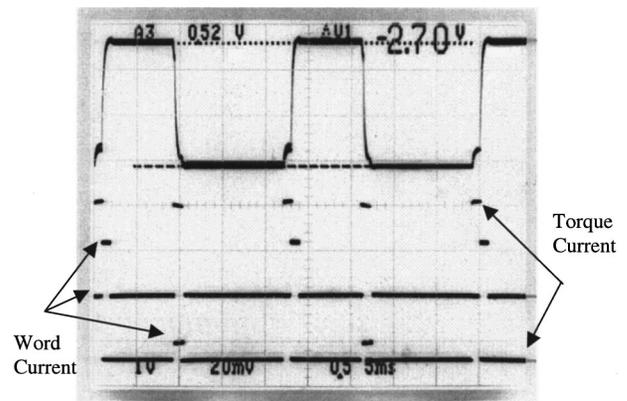


FIG. 6. Switching and latching characteristics of the SDT latch cell tested similarly as shown in Fig. 5, with an additional pulsed torque current. The word and torque currents are marked in the figure. The top wave form is the sense voltage signal from the two legs of SDT resistors using a  $50 \mu\text{A}$  sense current source. Torque current alone causes only minor change in the sense signal. The combination of the word and torque currents causes full switching.

cell. Faster external electronics will be needed to test the high-speed switching behavior of the SDT cells. The switching time is expected to be as short as 1 ns for SDT cells with a low RAP.<sup>7</sup>

#### IV. SUMMARY

Spin dependent tunneling junctions with latch configurations for memory applications were fabricated using rf diode sputtering and photolithography patterning. Basic latching functionality has been demonstrated using an external electronics setup. Compared with other MRAM technologies,<sup>8</sup> the output signal is high and the current required to write is reasonably low. This mode of operation shows high potential for memory applications because of its low power consumption for reading, the capability of rewriting, high speed, and nonvolatility.

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